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Fundamentals of Electronics

Book 2: Amplifiers: Analysis and Design

Thomas F. Schubert, Jr.
Ernest M. Kim

SYNTHESIS LECTURES ON DIGITAL CIRCUITS AND SYSTEMS

Mitchell A. Thornton, *Series Editor*

Fundamentals of Electronics
Book 2
Amplifiers: Analysis and Design

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Fundamentals of Electronics
Book 2
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SYNTHESIS LECTURES ON DIGITAL CIRCUITS AND SYSTEMS #47

MORGAN & CLAYPOOL PUBLISHERS

ABSTRACT

This book, *Amplifiers: Analysis and Design*, is the second of four books of a larger work, *Fundamentals of Electronics.* It is comprised of four chapters that describe the fundamentals of amplifier performance. Beginning with a review of two-port analysis, the first chapter introduces the modeling of the response of transistors to AC signals. Basic one-transistor amplifiers are extensively discussed. The next chapter expands the discussion to multiple transistor amplifiers. The coverage of simple amplifiers is concluded with a chapter that examines power amplifiers. This discussion defines the limits of small-signal analysis and explores the realm where these simplifying assumptions are no longer valid and distortion becomes present. The final chapter concludes the book with the first of two chapters in *Fundamental of Electronics* on the significant topic of feedback amplifiers.

Fundamentals of Electronics has been designed primarily for use in an upper division course in electronics for electrical engineering students. Typically such a course spans a full academic years consisting of two semesters or three quarters. As such, *Amplifiers: Analysis and Design,* and two other books, *Electronic Devices and Circuit Applications,* and *Active Filters and Amplifier Frequency Response*, form an appropriate body of material for such a course. Secondary applications include the use with *Electronic Devices and Circuit Applications* in a one-semester electronics course for engineers or as a reference for practicing engineers.

KEYWORDS

active loads, amplifier configurations, amplifiers, cascaded amplifiers, cascode, current mirror, current sources, Darlington amplifiers, distortion, feedback amplifiers, feedback topologies: shunt-series feedback, series-series feedback, series-shunt feedback, shunt-shunt feedback; gain, multistage amplifiers, optimal biasing, power amplifiers: class A, class B, class AB, push-pull; return difference, transistor modeling, two-port networks: *h*-parameters, *g*-parameters, *z*-paramters, *y*-parameters; thermal modeling

Contents

Preface

The basic principles of the operation of the four basic active elements, as described in Book 1, provide a good foundation for further study of electronic circuitry. Analog amplifiers constitute a major class of electronic circuitry and are a primary component in many applications. While it has been shown that electronic devices are basically non-linear, amplifiers typically operate within a region of incremental linearity. That is, a region where small variation in the input produces linearly amplified variation in the output. Analysis of such systems uses the principle of superposition: DC (or bias) conditions are separated from the AC (or variational) components of the input and output of an amplifier. The term "small-signal analysis" refers the use of linear models. "Large-signal analysis" implies operation near the transition between operational regions of an active device: such large-signal operation is typically non-linear and leads to distorted amplification.

This book begins with a review of two-port analysis. This review provides a basis for modeling transistors: they are most commonly modeled as two-port networks for small-signal analysis. At low frequencies the BJT is modeled by an *h*-parameter two-port and the FET as a modified hybrid- two-port. Simple amplifiers are approached by observing the previously observed region of operation that appeared between the two logic states of an inverter. All single-transistor amplifier configurations are analyzed and performance characteristics compared.

Multiple transistor amplifier circuitry is initially approached through cascading single transistor amplifiers using capacitive coupling. Only after the basic concepts are mastered, are the more complex circuits studied. Compound transistor configurations, such as the Darlington circuit, and direct-coupled amplifier stages are studied. As with single-transistor amplifiers, the previously observed linear region in ECL logic circuits leads to the study of emitter-coupled and source-coupled amplifiers. Common integrated circuit practices such as current source biasing and active loads are discussed.

Power amplifiers provide a good counterexample to the use of small-signal analysis. By necessity, the output of a power amplifier is not small and consequently may contain distorted components. Both harmonic and intermodulation distortion analysis techniques are introduced and compared. Amplifier conversion efficiency is discussed for class A, B, and AB power amplifiers. Thermal considerations are presented using simple heat transfer models and are related to power amplifier design criteria and limitations.

Feedback principles are introduced initially as a technique to stabilize amplifier gain, reduce distortion, and control impedance. The various configurations are introduced and analyzed

through two-port network analysis techniques. Improvement in frequency response is mentioned as an additional benefit but discussion is left for the next book in this series.

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October 2015

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In the development of any book, it seems that an infinite number of people provide and incalculable amount of guidance and help. While our thanks goes out to all those who helped, us, we can only mention a few of our many benefactors here. Special thanks go to Lynn Cox, who sparked our interest in writing an electronics text and, of course, to the staff at Morgan and Claypool Publishers, specifically Joe Claypool and Dr. C.L. Tondo.

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CHAPTER 5

Single Transistor Amplifiers

Circuits containing single Bipolar Junction and Field Effect Transistors are capable of providing amplification in six basic configurations: three configurations for each type of transistor. In the common-emitter and common-collector configurations for BJTs, the input signal is injected at the base of the transistor: in the common-base configuration it is injected at the emitter. Similarly, FET configurations have the input injected in the gate for common-source and common-drain configurations, and at the source for the common-gate configuration. These six single-transistor configurations are basic building blocks of amplifier design.

The focus of attention in this chapter is on the significant performance characteristics of each amplifier configuration: the voltage gain, current gain, input resistance and output resistance. Each configuration has a unique set of performance characteristics that are dependent on the transistor characteristics as well as the configuration and value of surrounding circuit elements. This chapter primarily investigates discrete amplifiers where biasing is accomplished with voltage sources and resistances: later chapters will highlight BJT biasing with current sources as developed in Section 3.6 (Book 1). The performance of transistor amplifiers with current source biasing can be directly derived from the results presented in this chapter. The frequency range of interest is the socalled midband region: that range of frequencies below where the transistor characteristics begin to change with increasing frequency and above where any capacitive elements (many circuits have *no* capacitors and therefore the midband frequency range begins at DC) have significant effect on the circuit performance

Although amplifiers are usually comprised of more than one amplification stage, at least one of these six configurations is contained as an amplification stage in nearly every amplifier. The properties derived here form a solid foundation for the analysis and design of multistage amplifiers presented in later chapters.

5.1 REVIEW OF TWO-PORT NETWORK BASICS

Electronic amplifiers are a subset of the system class commonly identified as *two-port networks*. In a two-port electronic network, signals are fed into a pair of terminals, amplified and/or modified by the system, and finally extracted at another pair of terminals. Each pair of terminals is identified as a port: signals are fed into an *input port* and extracted from an *output port*. The modeling and analysis of transistor-based amplifiers as well as feedback systems[1] is greatly simplified through the use of two-port network principles.

[1]The interconnection of two-port networks as used in the analysis of feedback amplifiers will be discussed in Chapter 8 (Book 2).

The items of interest in an electronic two-port network are the relationships between input port and output port voltages and currents. There are a few restrictions, upon which two-port analysis techniques are based, that must be identified:

- The network must be linear and time invariant.
- External connections may be made only to port terminals: no external connections can be made to any node internal to the port.
- All current entering one terminal of a port must exit the other terminal of that port.
- Sources and loads must be connected directly across the two terminals of a port.

Given the highly non-linear behavior of transistors, it may seem unusual to attempt to use two-port network analysis to describe transistor systems. It is possible, under small-signal conditions, however, to adequately model non-linear systems as *incrementally* linear. Electronic circuits previously discussed in this text have shown, along with non-linear operation, regions of linear operation. It is within these regions of linear operation that two-port analysis proves a particularly useful technique for the modeling of electronic systems.

As with all electronic systems, it is important to define sign conventions: Figure 5.1 is a representation of a two-port network with appropriate voltage and current polarity definitions. As is standard in electronic systems, the voltage and current at each port obey the passive sign convention. Typically, the input port is identified as port #1 and the output port as port #2.[2]

Three-terminal devices, such as transistors, can also be modeled using two-port techniques. One terminal is selected as a common terminal: that terminal is extended to both of the ports and becomes the reference (negative) terminal to each port.

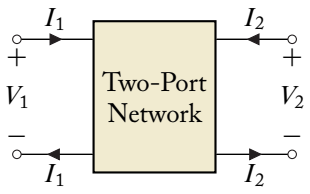


Figure 5.1: Two-port network sign conventions.

There are six basic sets of equivalent descriptive parameters for every two-port network:

1. Impedance parameters (z-parameters)—port voltages in terms of port currents.

[2]The numbering of ports is not universal in acceptance. It does, however, allow for simple notation in the description of the parameters relating currents and voltages. In some electronic two-port descriptions of systems, the numbering system is replaced by a more descriptive identification of parameters. One common example of descriptive notation occurs in *h*-parameter modeling of Bipolar Junction Transistors as presented in Section 5.2.

2. Admittance parameters (y-parameters)—port currents in terms of port voltages.

3. Hybrid parameters (h-parameters)—input voltage and output current in terms of input current and output voltage.

4. Hybrid parameters (g-parameters)—input current and output voltage in terms of input voltage and output current.

5. Transmission parameters ($ABCD$-parameters)—input current and voltage in terms of output current and voltage.

6. Transmission parameters (***ABCD***-parameters)—output current and voltage in terms of input current and voltage.

The first four of these sets are of particular interest in the study of electronic feedback systems, set numbers three and four (hybrid parameters) are often used in the description of transistor properties, and the last two sets of parameters are particularly useful in the study of communication transmission systems. A short description of the first four two-port parameter set descriptions follows.

Impedance parameters (z-parameters) The independent variables for this set of parameters are the port currents and the dependent variables are the port voltages: voltage as a function of current is an impedance. It is most common to write the equations in matrix form:

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} z_{11} & z_{12} \\ z_{21} & z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}. \tag{5.1}$$

The parameters $\{z_{ij}\}$ are called the impedance (or z-) parameters of the network. For a linear, time-invariant network, the z-parameters can be obtained by performing simple tests on the network:

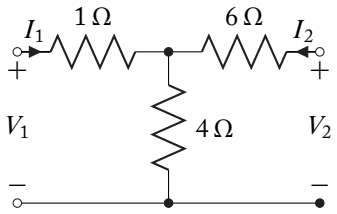
$$z_{ij} = \frac{V_i}{I_j} \Big|_{I_{k\neq j}=0} . \tag{5.2}$$

For a non-linear system that is operating in a region of linearity, a similar definition holds:

$$z_{ij} = \frac{\partial V_i}{\partial I_j} \Big|_{I_{k\neq j}=\text{Constant}} , \tag{5.3}$$

where the constant value of I_k is taken near the midpoint of the region of linearity. If a quiescent (zero-input) point exists, the constant value of I_k is chosen as its quiescent value.

Example 5.1
Determine the z-parameters for the given two-port network.



Solution:

The z-parameters are defined for this linear system as open-circuit parameters: one of the currents is always set to zero. Zero current implies an open circuit in the appropriate path. Thus:

$z_{11} = 1 + 4 = 5\,\Omega$ (zero current in the 6 Ω resistor)
$z_{12} = 4\,\Omega$ (no voltage drop across the 1 Ω resistor)
$z_{21} = 4\,\Omega$ (no voltage drop across the 6 Ω resistor)
$z_{22} = 6 + 4 = 10\,\Omega$ (zero current in the 1 Ω resistor)

Admittance parameters (y-parameters) Admittance parameters are defined with the independent variables are the port voltages and the dependent variables are the port currents: current as a function of voltage carries the units of admittance. The y-parameter equations are:

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \tag{5.4}$$

The parameters can be determined by performing the tests:

$$y_{ij} = \frac{I_i}{V_j}\Big|_{V_{k\neq j}=0}, \tag{5.5}$$

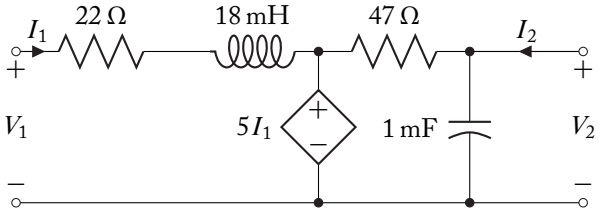
or

$$y_{ij} = \frac{\partial I_i}{\partial V_j}\Big|_{V_{k\neq j}=\text{Constant}}. \tag{5.6}$$

In a linear system the test for finding y-parameters indicates that a voltage must be set to zero: thus, the parameters are often called *short-circuit* admittance parameters.

Example 5.2

Determine the y-parameters for the network shown using standard phasor techniques, that is, find $Y(s)$.



Solution:

It can be seen that this network is a linear system. Both two-port and phasor techniques are appropriate for such a system. The phasor equivalent impedance of the inductor and the capacitor are:

$$Z_L = 0.018\,\text{s} \qquad Z_C = 1000/\text{s}.$$

The y-parameter tests for a linear system are given by Equation (5.5):

$$y_{ij} = \frac{I_i}{V_j}\Big|_{V_{k\neq j}=0}.$$

In order to solve for y_{11} and y_{21}, the output terminals are short-circuited ($V_2 = 0$). A loop equation can then be written around the remaining left loop:

$$V_1 - 22I_1 - 0.018\,\text{s}\,I_1 - 5I_1 = 0.$$

Which leads to:

$$y_{11} = \frac{I_1}{V_1}\bigg|_{V_2=0} = \frac{1}{27 + 0.018\,\text{s}}.$$

Since the capacitor has been shorted out by setting $V_2 = 0$, a loop equation can be written around the remaining right loop:

$$5I_1 + 47I_2 = 0 \quad \Rightarrow \quad I_2 = -0.1064I_1,$$

and

$$y_{21} = \frac{I_2}{V_1}\bigg|_{V_2=0} = \frac{1}{253 + 0.1692\,\text{s}}.$$

The other two parameters, y_{12} and y_{22}, are obtained by shorting the input terminal ($V_1 = 0$). A loop equation around the left loop of this configuration yields:

$$22I_1 + 0.018\,\text{s}I_1 - 5I_1 = 0 \quad \Rightarrow \quad I_1 = 0.$$

Obviously

$$y_{12} = \frac{I_1}{V_2}\bigg|_{V_1=0} = 0.$$

With $I_1 = 0$, the current I_2 is the sum of the currents in the 47 Ω resistor and the capacitor (the dependent voltage source has zero value):

$$y_{22} = \left.\frac{I_2}{V_2}\right|_{V_1=0} = y_{47\,\Omega} + y_{1\,\mathrm{mF}} = 0.02128 + 0.001\,\mathrm{s}.$$

The y-parameter matrix is then given by:

$$Y(s) = \begin{bmatrix} \dfrac{1}{27 + 0.018\,\mathrm{s}} & 0 \\ \dfrac{1}{253 + 0.1692\,\mathrm{s}} & 0.02128 + 0.001\,\mathrm{s} \end{bmatrix}.$$

Hybrid parameters (h-parameters) The independent variables are the input voltage and output current; the dependent variables are the input current and output voltage.

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}. \tag{5.7}$$

Notice that these parameters, unlike the z- and y-parameters, do not all have the same dimensions. Each is different: h_{11} is the input port impedance; h_{12} is a dimensionless (input over output) voltage ratio; h_{21} is a dimensionless (output over input) current ratio; and h_{22} is output port admittance.

The parameters can be determined by performing the tests:

$$\begin{aligned} h_{11} &= \left.\frac{V_1}{I_1}\right|_{V_2=0} & h_{12} &= \left.\frac{V_1}{V_2}\right|_{I_1=0} \\ h_{21} &= \left.\frac{I_2}{I_1}\right|_{V_2=0} & h_{22} &= \left.\frac{I_2}{V_2}\right|_{I_1=0} \end{aligned} \tag{5.8}$$

or

$$\begin{aligned} h_{11} &= \left.\frac{\partial V_1}{\partial I_1}\right|_{V_2=\mathrm{Constant}} & h_{12} &= \left.\frac{\partial V_1}{\partial V_2}\right|_{I_1=\mathrm{Constant}} \\ h_{21} &= \left.\frac{\partial I_2}{\partial I_1}\right|_{V_2=\mathrm{Constant}} & h_{22} &= \left.\frac{\partial I_2}{\partial V_2}\right|_{I_1=\mathrm{Constant}}. \end{aligned} \tag{5.9}$$

Hybrid parameters (g-parameters) The independent variables are the input current and output voltage; the dependent variables are the input voltage and output current.

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}. \tag{5.10}$$

Notice that these parameters, like the h-parameters, do not all have the same dimensions. Each is different: g_{11} is the input port admittance; g_{12} is a dimensionless (input over output) current ratio; g_{21} is a dimensionless (output over input) voltage ratio; and g_{22} is output port impedance.

The parameters can be determined by performing the tests:

$$\begin{aligned} g_{11} &= \left.\frac{I_1}{V_1}\right|_{I_2=0} & g_{12} &= \left.\frac{I_1}{I_2}\right|_{V_1=0} \\ g_{21} &= \left.\frac{V_2}{V_1}\right|_{I_2=0} & g_{22} &= \left.\frac{V_2}{I_2}\right|_{V_1=0} \end{aligned} \tag{5.11}$$

or

$$\begin{aligned} g_{11} &= \left.\frac{\partial I_1}{\partial V_1}\right|_{I_2=\text{Constant}} & g_{12} &= \left.\frac{\partial I_1}{\partial I_2}\right|_{V_1=\text{Constant}} \\ g_{21} &= \left.\frac{\partial V_2}{\partial V_1}\right|_{I_2=\text{Constant}} & g_{22} &= \left.\frac{\partial V_2}{\partial I_2}\right|_{V_1=\text{Constant}} \end{aligned} . \tag{5.12}$$

5.1.1 CIRCUIT REPRESENTATION OF A TWO-PORT NETWORK

It is often important to create a simple equivalent circuit for a two-port network where the network parameters are known. While there are several techniques for the creation of these equivalent networks, the most useful in electronic applications involves Thévenin and Norton input and output realizations. In general, network parameters are replaced by simple circuit elements as shown in Table 5.1. Relationships between currents and voltages at the same port are treated as impedances or admittances, while relationships at different ports are treated as dependent sources.

Table 5.1: Two-port network replacement circuit elements for network parameters

Network Parameter	Replacement Circuit Element	
	Same Port	Opposite Port
impedance	impedance	current-controlled voltage source
admittance	admittance	voltage-controlled current source
current ratio	(not applicable)	current-controlled current source
voltage ratio	(not applicable)	voltage-controlled voltage source

Example 5.3

A two-port network has been found to have the following g-parameters:

$$\begin{aligned} g_{11} &= 0.025\,\text{S} & g_{12} &= 47\,\text{mA/A} \\ g_{21} &= 14\,\text{V/V} & g_{22} &= 270\,\Omega . \end{aligned}$$

Determine an equivalent circuit representation of the two-port network.

Solution:

The matrix equation for the g-parameter representation of a two-port network can be written as two separate equations:

$$I_1 = g_{11}V_1 + g_{21}I_2 \quad \text{and} \quad V_2 = g_{21}V_1 + g_{22}I_2.$$

The equation for I_1 reveals that two currents must be added together to make the input port current. Referring to Table 5.1, one finds that the currents emanate from an admittance and a current-controlled current source: they must be connected as a Norton source. The equation for V_2 implies that two voltages must be added together. Table 5.1 shows the elements are an impedance and a voltage-controlled voltage source: they are connected in Thévenin fashion. The equivalent circuit representation is shown in Figure 5.2 (Note: for clarity, g_{11} is shown as a resistance rather than a conductance).

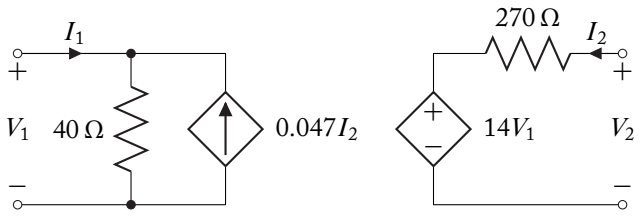


Figure 5.2: Two-port realization of Example 5.3.

5.2 BJT LOW-FREQUENCY MODELS

In previous sections it has been shown that the Ebers-Moll model is an effective model in all regions of Bipolar Junction Transistor operation. It has also been shown that for large-signal behavior, a simplified set of models can bring additional insight into the operation of an electronic circuit. These models are first-order approximations to BJT operation, and exhibit some degree of error. When a BJT is operating in the forward-active region, it is appropriate to improve the modeling of its operation with a second-order approximation. As in most series approximations to behavior, second-order effects are a linearization, about the first-order (in this case, the quiescent) behavior, and are therefore added to the first-order behavior.

In the case of BJT operation, small-signal (often called AC) variations are linearized approximates to the operation of a transistor about its large-signal (often called DC or quiescent) behavior. Previous discussions of Bipolar Junction Transistors[3] have shown that the forward-active region (and, similarly, the inverse-active region) of BJT operation are approximately linear

[3]See Section 3.5 (Book 1)—Digital Applications. In particular, discussions of the transfer relationship for the logic inverter and ECL logic OR gate showed a linear transition region between the two logic levels. These transition regions occurred when the BJT was operating in the forward-active region in transition between the cut-off and saturation regions.

in nature. It is therefore quite reasonable to assume that small-signal approximations have great validity in the modeling of BJT operation. The small-signal approximations are made in the form of approximate models that take the form of two-port networks. Two-port network characterizations are valid for non-linear systems that have regions of linearity: the BJT operating in either of its active regions is such a system.

The first obvious problem in modeling a BJT as a two-port is that there are only three terminals rather than the four that seem to be necessary. This obstacle is overcome by assigning one BJT terminal *common* to both ports. Practice has made two possibilities for this common terminal standard: either the emitter or the base are chosen to be the common terminal. In Figure 5.3, an *npn* BJT is shown as a two-port network with the emitter terminal chosen as common. In Chapter 3 (Book 1), it was shown that the major controlling port of a BJT is the base-emitter junction. Thus, the port containing the base-emitter junction is considered the input port and the remaining port (which contains the collector terminal and the common terminal), the output port. Since the terminal voltages and currents for BJTs have previously been identified with subscripts that are descriptive rather than the general numerical form of Section 5.1, the descriptive subscripts will be continued in the BJT two-port representation.

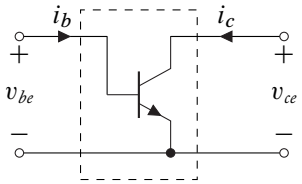


Figure 5.3: A bipolar junction transistor as a two-port network (emitter as common terminal).

The modeling process for transistor circuit performance is:

1. Model the BJT with an appropriate DC model.
2. Determine the circuit quiescent (DC) conditions—verify BJT active region.
3. Determine the BJT AC model parameters from the quiescent conditions.
4. Create an AC equivalent circuit.
5. Determine the circuit AC performance by:
   (a) replacing the BJT by its AC model, or
   (b) using previously derived results for the circuit topology.
6. Add the results of the DC and AC analysis to obtain total circuit performance.

Techniques for the DC modeling of BJTs and the determination of quiescent conditions have been discussed thoroughly in Chapter 3 (Book 1): discussions of AC modeling follow. The steps relating to circuit performance are discussed in later sections of this chapter.

The choice of which set of two-port parameters will be most helpful in the modeling of a BJT is important. One good starting point is the Ebers-Moll model. The Ebers-Moll model for an *npn* BJT is shown in Figure 5.4.

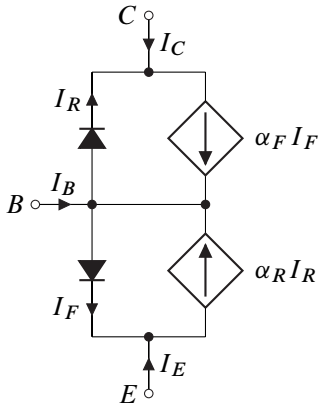


Figure 5.4: The Ebers-Moll model of an *npn* BJT.

In the forward-active region of operation, the base-emitter junction is forward-biased and the base-collector junction is reverse biased. Approximate models[4] for forward-biased and reverse-biased diodes lead to the base-collector junction diode taking on the appearance of a very large resistance, while the base-emitter junction diode can be linearized about the quiescent point to a much smaller resistance. The forward current source (described by α_F) remains significant while the reverse current source supplies very little current. This small-signal model is shown in Figure 5.5, with the two junction dynamic resistances defined as:

$$r_{df} = \text{base-emitter diode forward dynamic resistance,}$$
$$r_{dr} = \text{base-collector diode dynamic reverse resistance.}$$

The dynamic resistance of a junction was derived in Chapter 2 (Book 1) to be:

$$r_d = \frac{\partial V}{\partial I} = \frac{\eta V_t}{I_s + I} = \frac{\eta V_t}{I_s} e^{-\frac{V}{\eta V_t}}. \tag{5.13}$$

The forward-biased value of this dynamic resistance is strongly dependent on the quiescent conditions, while the reverse-biased value is, in an active-region BJT, not. Thus, r_{df} is strongly de-

[4]Models of a diode were derived in Chapter 2 (Book 1). The forward-biased biased model also includes a DC voltage source. The presence of that DC voltage source only affects quiescent behavior and not small signal (AC) behavior. For that reason it is eliminated in these discussions.

pendent on the quiescent conditions while r_{dr}, a much larger value, is not. While the derivation of this small-signal model was based on the Ebers-Moll model of an *npn* BJT, the small-signal model itself is valid for *both npn* and *pnp* BJTs. Reversing the direction of the junctions only changes quiescent conditions, it does not change the expressions for dynamic resistance.

The analysis of electronic systems could be implemented using the model of Figure 5.5, however two-port techniques simplify many aspects of analysis. The two-port realization of

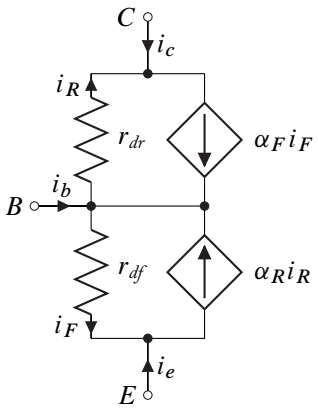


Figure 5.5: A forward-active small-signal model of a BJT.

such a system would most effectively be accomplished by an *h*-parameter representation. This *h*-parameter realization is a common representation for small-signal, low-frequency BJT operation.[5] Figure 5.6 shows the *h*-parameter realization of a small-signal model of a BJT.

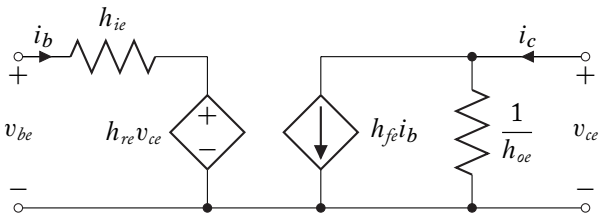


Figure 5.6: The common-emitter *h*-parameter model for a BJT.

[5]Other possible models include the T-model and the hybrid-π model. The *h*-parameter model is chosen as an introductory small-signal model for its simplicity. The hybrid-π model will be introduced in Chapter 10 (Book 3) where its added complexity is necessary to adequately describe frequency-dependent effects.

The governing equations[6] for the h-parameter model are:

$$v_{be} = h_{ie} i_b + h_{re} v_{ce} \tag{5.14a}$$

and

$$i_c = h_{fe} i_b + h_{oe} v_{ce} \tag{5.14b}$$

where descriptive subscripts have been chosen for the subscripts of the h-parameters. The second subscript defines which terminal is chosen as common (either the base or the emitter), and the first subscript identifies the function of the parameter:

$$\begin{aligned} h_{ie} &= \text{input impedance—emitter as common terminal} \\ h_{re} &= \text{reverse voltage gain—emitter as common terminal} \\ h_{fe} &= \text{forward current gain—emitter as common terminal} \\ h_{oe} &= \text{output admittance—emitter as common terminal.} \end{aligned}$$

The parameters[7] can be found as:

$$\begin{aligned} h_{ie} &= \left.\frac{\partial V_{BE}}{\partial I_b}\right|_{V_{CE}=V_{CEq}} & h_{re} &= \left.\frac{\partial V_{BE}}{\partial V_{CE}}\right|_{I_B=I_{Bq}} \\ h_{fe} &= \left.\frac{\partial I_C}{\partial I_B}\right|_{V_{CE}=V_{CEq}} & h_{oe} &= \left.\frac{\partial I_C}{\partial V_{CE}}\right|_{I_B=I_{Bq}}. \end{aligned} \tag{5.15}$$

Equations (5.15) can be revised using AC voltages and currents. Realizing that AC signals are variations about the quiescent point and that constant values have zero AC component, the h-parameters can also be defined as:

$$\begin{aligned} h_{ie} &= \left.\frac{v_{be}}{i_b}\right|_{v_{ce}=0} & h_{re} &= \left.\frac{v_{be}}{v_{ce}}\right|_{i_b=0} \\ h_{fe} &= \left.\frac{i_c}{i_b}\right|_{v_{ce}=0} & h_{oe} &= \left.\frac{i_c}{v_{ce}}\right|_{i_b=0}. \end{aligned} \tag{5.16}$$

All the signals in Equation (5.16) are AC signals. Setting an AC signal (i.e., i_b or v_{ce}) to zero holds the AC variation of that signal to zero, it does not change the quiescent conditions of the BJT.

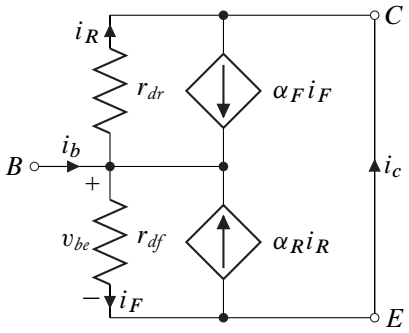
Determination of the small-signal BJT h-parameters is accomplished by applying Equations (5.16) to the circuit of Figure 5.5.

[6]Small letters with small subscripts indicate that these parameters are AC (or small-signal) parameters. They are a linearization of the transistor characteristics about a quiescent point and therefore depend on that quiescent point.

[7]The final subscript "q" indicates the quiescent value of the circuit parameter. Thus, I_{Bq} and V_{CEq} are the quiescent (DC) values of the base current and the collector-emitter voltage for the transistor.

5.2.1 DETERMINATION OF h_{ie} AND h_{fe}

The determination of these two parameters necessitates that the collector and emitter terminals be shorted, according to the requirements of Equation (5.16), in an AC sense. A DC quiescent current flows the quiescent collector-emitter voltage is greater than $V_{CE(sat)}$ and the BJT is in the forward-active region.



The small-signal ratios can be obtained by applying Kirchhoff's current law applied at the base node:

$$i_b = i_F\,(1-\alpha_F) + i_R\,(1-\alpha_R)\,, \tag{5.17}$$

where

$$i_F = \frac{v_{be}}{r_{df}} \quad \text{and} \quad i_R = \frac{v_{be}}{r_{dr}}. \tag{5.18}$$

The relationships of (5.18) inserted into Equation (5.17) yield:

$$i_b = \frac{v_{be}}{r_{df}}\,(1-\alpha_F) + \frac{v_{be}}{r_{dr}}\,(1-\alpha_R)\,. \tag{5.19}$$

Equation (5.19) directly leads to the first of the h-parameters. The relative size of the forward and reverse dynamic resistances of the junctions, $r_{dr} \gg r_{df}$, leads to a simplified expression for h_{ie}:

$$h_{ie} = \frac{v_{be}}{i_b} = \left(\frac{r_{df}}{1-\alpha_F}\right) // \left(\frac{r_{dr}}{1-\alpha_R}\right) \approx \frac{r_{df}}{1-\alpha_F} = (\beta_F + 1)\,r_{df}. \tag{5.20}$$

The value for h_{ie} is dependent on r_{df}, a quantity that strongly depends on the quiescent conditions: h_{ie} must also strongly depend on quiescent conditions. Equation (5.13) can be used to obtain and expression for h_{ie} in terms of the quiescent collector current and $\eta V_t \approx 26\,\text{mV}$:

$$h_{ie} \approx (\beta_F + 1)\,\frac{\eta V_t}{I + I_S} \approx (\beta_F + 1)\,\frac{\eta V_t}{|I_C|}. \tag{5.21}$$

An additional equation must be written to find h_{fe}. At the collector node Kirchhoff's Current Law gives:

$$i_c = \alpha_F i_F - i_R = \alpha_F \frac{v_{be}}{r_{df}} - \frac{v_{be}}{r_{dr}}, \tag{5.22}$$

which, noting the relative dynamic resistance sizes, can be reduced to

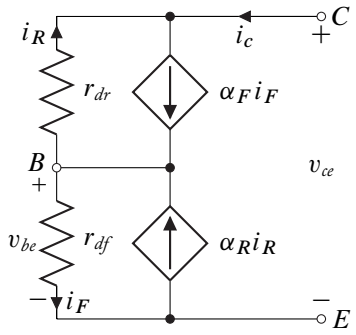
$$\frac{v_{be}}{i_c} = \left(\frac{r_{df}}{\alpha_F} // r_{dr} \right) \approx \frac{r_{df}}{\alpha_F}. \tag{5.23}$$

The required current ratio for h_{fe} is found using Equations (5.20) and (5.23):

$$h_{fe} = \frac{i_c}{i_b} \approx \frac{\dfrac{\alpha_F}{r_{df}}}{\dfrac{(1-\alpha_F)}{r_{df}}} = \beta_F. \tag{5.24}$$

5.2.2 DETERMINATION OF h_{re} AND h_{oe}

The tests for these two h-parameters (as seen in Equation (5.16)) require that the small-signal base current be set to zero. Again, remember that there is still a quiescent (DC) current flowing and the BJT is in the forward-active region. Kirchhoff's Current Law applied at the base node yields:



$$i_F\,(1-\alpha_F) + i_R\,(1-\alpha_R) = 0, \tag{5.25}$$

where,

$$i_F = \frac{v_{be}}{r_{df}} \qquad \text{and} \qquad i_R = \frac{v_{be} - v_{ce}}{r_{dr}}. \tag{5.26}$$

Then inserting (5.26) into (5.25) yields

$$\frac{v_{be}}{r_{df}}(1-\alpha_F) + \frac{v_{be} - v_{ce}}{r_{dr}}(1-\alpha_R) = 0, \tag{5.27}$$

or

$$v_{be}\left(\frac{1-\alpha_F}{r_{df}}+\frac{1-\alpha_R}{r_{dr}}\right)=v_{ce}\left(\frac{1-\alpha_R}{r_{dr}}\right). \tag{5.28}$$

The required voltage ratio can now be determined as:

$$h_{re}=\frac{v_{be}}{v_{ce}}=\frac{\left(\frac{r_{df}}{1-\alpha_F}//\frac{r_{dr}}{1-\alpha_R}\right)}{\frac{r_{dr}}{1-\alpha_R}}\approx\frac{r_{df}}{r_{dr}}\left(\frac{1-\alpha_R}{1-\alpha_F}\right)=\frac{r_{df}}{r_{dr}}\left(\frac{1+\beta_F}{1+\beta_R}\right). \tag{5.29}$$

The value for h_{re} is seen to be a *very* small quantity and can safely be assumed to be zero in the modeling of a BJT in either active region. In order to solve for h_{oe}, Kirchhoff's Current Law is applied at the emitter node:

$$i_c=i_F-\alpha_R i_R=\frac{v_{be}}{r_{df}}-\alpha_F\frac{v_{be}-v_{ce}}{r_{dr}}=v_{be}\left(\frac{1}{r_{df}}-\frac{\alpha_F}{r_{dr}}\right)+\frac{v_{ce}}{r_{dr}}. \tag{5.30}$$

Again using the property that $r_{df}\ll r_{dr}$, a simplification can be made

$$i_c\approx\frac{v_{be}}{r_{df}}+\frac{v_{ce}}{r_{dr}}. \tag{5.31}$$

Equation (5.29) can be used to eliminate v_{be} from Equation (5.31):

$$i_c\approx\frac{v_{ce}}{r_{df}}\frac{r_{df}}{r_{dr}}\left(\frac{1-\alpha_R}{1-\alpha_F}\right)+\frac{v_{ce}}{r_{dr}}=\frac{v_{ce}}{r_{dr}}\left(\frac{1+\beta_F}{1+\beta_R}+1\right). \tag{5.32}$$

The relationship for h_{oe} is obtained from Equation (5.32):

$$h_{oe}=\frac{i_c}{v_{ce}}\approx\frac{1}{r_{dr}}\left(\frac{1+\beta_F}{1+\beta_R}+1\right). \tag{5.33}$$

This is a very small output conductance (the equivalent of a very large output resistance). The simplified expression of Equation (5.33) does not adequately model all the resistances contributing to output resistance for a real BJT. The actual output resistance is much smaller that is predicted by the Ebers-Moll model. A more accurate predictor of the output resistance, r_o, is defined in terms of another quantity, the early voltage, V_A.[8]

$$\frac{1}{h_{oe}}=r_o=\left|\frac{V_A}{I_C}\right|. \tag{5.34}$$

[8]The early voltage is a parameter that describes the change in the width of the base region of a BJT which results from a change in base-collector junction voltage. A basic description of the effect can be found in most solid state electronics texts, but is beyond the scope of this text.

The early voltage for a BJT is usually determined experimentally by observing the slope of the I_C vs. V_{CE} curves for a BJT in the forward-active region. It typically has a value of 100 V or more and is defined as:

$$V_A = \frac{I_C}{\frac{\partial I_C}{\partial V_{CE}}}. \tag{5.35}$$

This output resistance is often large compared to the resistances connected to the collector-emitter port of the BJT and h_{oe} can, in that case, be assumed approximately equal to zero. When the external resistances are not small compared to the output resistance it is necessary to include h_{oe} in the model for the BJT.

The h-parameters for a BJT are summarized in Table 5.2. Only one parameter, h_{fe}, is essentially independent of quiescent conditions, while the other three parameters depend to varying degrees on the bias conditions, specifically on the quiescent collector current, I_C.

Table 5.2: BJT h-parameter summary

h-Parameter	Value
h_{ie}	$\approx (\beta_F + 1)\frac{\eta V_t}{\lvert I_C \rvert}$
h_{fe}	$\approx \beta_F$
h_{re}	$\approx \frac{r_{df}}{r_{dr}}\left(\frac{1+\beta_F}{1+\beta_R}\right) \approx 0$
h_{oe}	$= \left\lvert \frac{I_C}{V_A} \right\rvert \approx 0$

The extremely small values of h_{re} and h_{oe} lead to a simplified h-parameter model of a BJT where these two parameters are assumed to be approximately zero, as shown in Figure 5.7. When large resistances are connected to the collector-emitter port of the BJT it is important to reintroduce h_{oe} into the h-parameter model as a conductance shunting the dependent current source. In typical BJT applications, h_{re} is not significant.

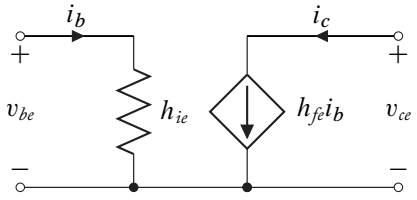
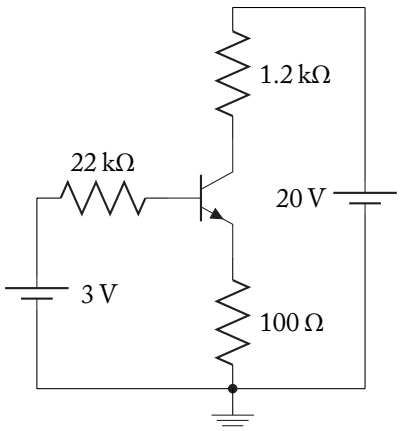


Figure 5.7: Simplified small-signal h-parameter model for a BJT.

Example 5.4
Given a Silicon *npn* BJT with parameters:

$$\beta_F = 150 \qquad V_A = 350\,\text{V},$$

operating in the given circuit at room temperature. Determine an appropriate small-signal *h*-parameter model for the BJT.



Solution:

The quiescent conditions must first be obtained: KCL taken around the base-emitter loop yields

$$3 - 22\,\text{k}I_B - 0.7 - 100(151I_B) = 0$$
$$I_B = 62.0\,\mu\text{A} \quad \text{and} \quad I_C = 150I_B = 9.30\,\text{mA}.$$

Checking to see if the BJT is in the forward-active region by using KCL around the collector-emitter loop yields:

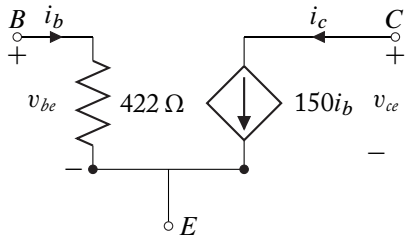
$$V_{CE} = 20 - 1.2\,\text{k}I_C - 100\left(\frac{151}{150}I_C\right) = 7.90\ \text{V}.$$

This value is greater than $V_{CE(sat)}$, which implies that the BJT is in the forward-active region and the *h*-parameter model parameters itemized in Table 5.2 may be used.

$$h_{fe} \approx \beta_F = 150$$
$$h_{ie} \approx (\beta_F + 1)\frac{\eta V_t}{|I_C|} = (151)\frac{26\,\text{mV}}{|9.30\,\text{mA}|} = 422\,\Omega$$
$$h_{oe} = \left|\frac{I_C}{V_A}\right| = \left|\frac{9.30\,\text{mA}}{350\,\text{V}}\right| = 26.6\,\mu\text{S} \approx 0$$
$$h_{re} \approx 0.$$

It is necessary to check to see if h_{oe} can be approximated as zero value. It is equivalent to a resistance, r_o, of 37.6 kΩ (the resistance is the inverse of h_{oe}), which is large with respect to the 1.2 kΩ and 100 Ω resistors connected to the collector-emitter port of the BJT: h_{oe} can be assumed in this application to be approximately zero in value.

The approximate small-signal model of this BJT operating in this circuit is therefore found to be:



5.3 COMMON-EMITTER AMPLIFIERS

A description of the general performance of a common-emitter amplifier can be derived directly from the voltage transfer relationship of a BJT logic inverter. The BJT logic inverter, discussed in Section 3.5 (Book 1), has two distinct regions where the voltage output is relatively constant: when the BJT is in either the saturation or in cut-off region. Between these two regions lies a linear region where the variation in the output voltage about the quiescent point is directly proportional to the variation in the input voltage. This linear-region proportionality constant for the logic inverter was seen in Example 3.5-1 to be negative and greater than 1 in magnitude: the input signal variations were amplified and inverted. The discussions of Section 3.5 (Book 1) were based on coarse, first-order approximations of the operation of a BJT in each of its regions of operation. This section develops the characteristics of this type of amplifier (and its close relatives) using the second-order *h*-parameter approximations developed earlier in this chapter.

Common-emitter amplifiers have the same general circuit topology as the logic inverter:

- the input signal enters the BJT at the base,
- the output signal exits the BJT at the collector, and
- the emitter is connected to a constant voltage, often the ground (common) terminal, sometimes with an intervening resistor.

A simple common-emitter amplifier is shown in Figure 5.8. It is necessary that the quiescent point of the BJT be set with the circuitry external to the transistor so that it is in the forward-active region. The values of the resistors, R_c and R_s, and the DC voltage sources, V_{CC}

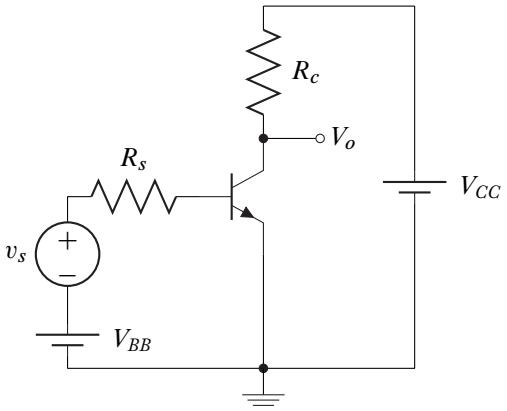


Figure 5.8: A simple common-emitter amplifier.

and V_{BB}, have therefore been chosen so that the BJT is in the forward-active region and the circuit will operate as an amplifier. The voltage source, v_s, is a small-signal AC source.

Once the circuit quiescent ($v_s = 0$) conditions have been calculated and it has been determined that the BJT is in the forward-active region of operation, the significant h-parameters can be calculated to form the small-signal model of the transistor:

$$\begin{aligned} h_{fe} &= \beta_F \qquad\qquad h_{oe} = \frac{I_c}{V_A} \approx 0. \\ h_{ie} &= (\beta_F + 1)\left|\frac{\eta V_t}{I_C}\right|. \end{aligned} \tag{5.36}$$

The small-signal (often called AC) circuit performance can now be calculated. Total circuit performance is the sum of quiescent and small-signal performance: the process is basically a superposition of the zero-frequency solution with the low-frequency AC solution.[9] In each case, solutions are formed by setting the independent sources at all other frequencies to zero. AC circuit performance is obtained through analysis of a circuit obtained by setting the original circuit DC sources to zero, and then replacing the BJT with its h-parameter two-port model. This circuit reconfiguration process, applied to Figure 5.8, is shown in Figure 5.9.

The small-signal performance characteristics[10] that are of interest in any amplifier are: *the current gain, the input resistance, the voltage gain,* and *the output resistance.* For the simple common-emitter amplifier under consideration, these characteristics can be obtained from analysis of the circuit of Figure 5.9b. Definitions for these quantities often vary due to differing definition of the exact location of the point of measurement. Care must always be taken to *ensure that measurement points are clearly understood before any analysis begins.*

[9] At high frequencies the BJT performance characteristics change. See Book 3.

[10] It should be remembered that the quantities discussed in this section and following sections are small-signal (or AC) quantities. The ratios considered here are the ratios of AC quantities not the ratios of total currents and/or voltages.

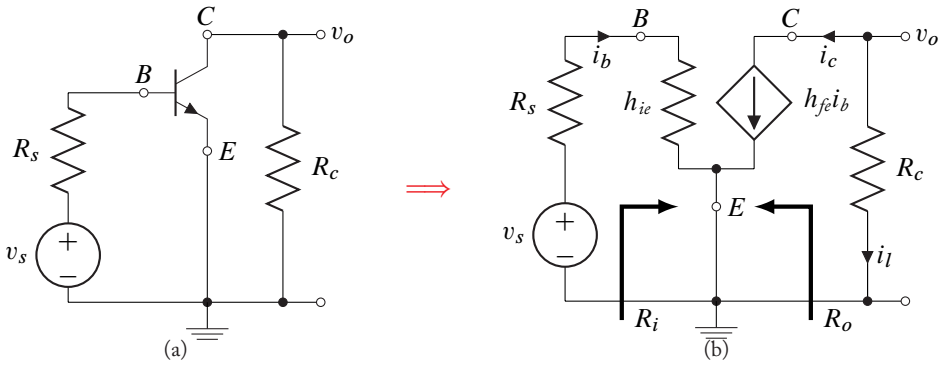


Figure 5.9: AC modelling of a simple common-emitter amplifier. (a) The small-signal circuit: DC sources set to zero; (b) BJT replaced by h-parameter model.

Current Gain

For this simple transistor amplifier, the current gain is defined as the ratio of load current to input current, that is:

$$A_I \equiv \frac{i_l}{i_b} = \frac{-i_c}{i_b}. \tag{5.37}$$

From the circuit of Figure 5.9b, it can easily be determined that the collector and base currents are related through the dependent current source by the constant h_{fe}. The current gain is dependent only on the BJT characteristics and independent of any other circuit element values. Its value is given by:

$$A_I = -h_{fe}, \tag{5.38}$$

where the negative sign implies that the small-signal current input is inverted as well as amplified. If the resistor R_c is large then the output resistance of the BJT must be considered in calculating the current gain. Including h_{oe} in the BJT h-parameter model divides the output current between the output resistance, $r_o = 1/h_{oe}$ and the collector resistance:

$$A_I = -h_{fe}\frac{r_o}{r_o + R_c}. \tag{5.39}$$

Input Resistance

Input resistance is measure of the AC input current as a function of the input voltage. If the AC input voltage, v_b, is taken at the input terminal of the BJT (the base), the input resistance (shown if Figure 5.9b with the bold arrow and labeled as R_i) is given by:

$$R_i \equiv \frac{v_b}{i_b} = h_{ie}. \tag{5.40}$$

The input resistance is unaffected by finite r_o.

Voltage Gain

The voltage gain is the ratio of output voltage to input voltage. If the input voltage is again taken to be the voltage at the input to the transistor, v_b, the voltage gain is defined as:

$$A_V \equiv \frac{v_o}{v_b}. \tag{5.41}$$

One of the best methods for obtaining this ratio is through the use of quantities already calculated or otherwise easily obtained:

$$A_V = \frac{v_o}{v_b} = \left(\frac{v_o}{i_l}\right)\left(\frac{i_l}{i_b}\right)\left(\frac{i_b}{v_b}\right). \tag{5.42}$$

The expressions for each quantity, when substituted into Equation (5.42), yield:

$$A_V = (R_c)\,(A_I)\left(\frac{1}{R_i}\right) = \frac{-h_{fe}R_c}{h_{ie}}. \tag{5.43}$$

Again, the small-signal output voltage is an inverted, amplified replica of the input voltage. The voltage gain can be very large in magnitude. Equation (5.43) indicates it is limited only by the BJT parameter h_{fe} and the external resistance R_c. That conclusion is based, however, on the assumption that R_c is small with respect to r_o. If R_c approaches the magnitude of r_o, the gain becomes limited by the output resistance of the amplifier, and R_c must be replaced by $R_c//r_o$ in Equation (5.43).

Often the voltage gain from the source to the load is of interest as well. This overall voltage gain can be defined as:

$$A_{VS} \equiv \frac{v_o}{v_s}. \tag{5.44}$$

This ratio can be directly derived from the simple voltage gain, A_V, with a voltage division using the amplifier input resistance and the source resistance:

$$A_{VS} = \frac{v_o}{v_s} = \left(\frac{v_o}{v_b}\right)\left(\frac{v_b}{v_s}\right) = A_V\left(\frac{R_i}{R_i + R_s}\right), \tag{5.45}$$

or

$$A_{VS} = \left(\frac{-h_{fe}R_c}{h_{ie}}\right)\left(\frac{h_{ie}}{h_{ie} + R_s}\right) = \frac{-h_{fe}R_c}{h_{ie} + R_s}. \tag{5.46}$$

Since A_{VS} is dependent on A_V it is also limited in magnitude by finite r_o. To include the effect of finite r_o, R_c must be replaced by $R_c//r_o$ in Equation (5.46).

Output Resistance

The output resistance is defined as the Thévenin resistance at the output of the amplifier (in this case the BJT collector) looking back into the amplifier. As in the case of voltage gain, the exact

point of measurement is not always clear. The arrow in circuit diagram of Figure 5.9 indicates that R_o is to be measured without considering R_c: it is also possible to define an output resistance, R_{ol}, that includes the effects of collector resistance, R_c. The AC equivalent circuit used to calculate the output resistance is shown in Figure 5.10a. The input independent source is set to zero and the Thévenin resistance is calculated looking into the output. It can easily be seen that $i_b = 0$ in this circuit. Kirchhoff's Voltage Law taken around the base loop gives:

$$i_b\,(h_{ie} + R_s) = 0 \qquad \Rightarrow \qquad i_b = 0.$$

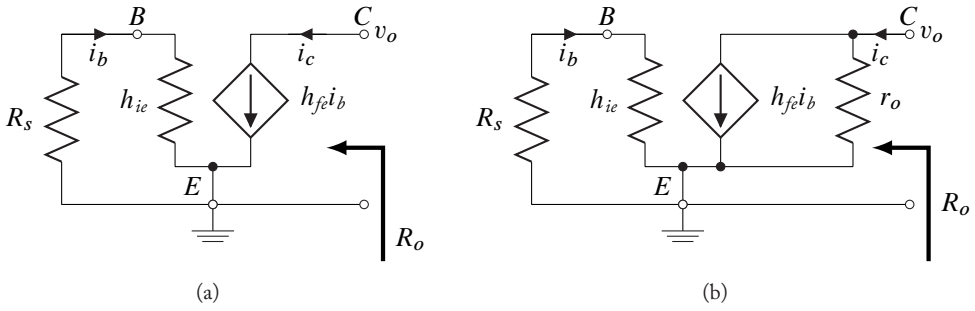


Figure 5.10: Circuit for calculation of output resistance. (a) Small-signal output circuit: AC source set to zero; (b) More accurate BJT h-parameter model.

Zero base current implies that the dependent current source is also zero-valued and the output resistance becomes:

$$R_o \approx \infty. \tag{5.47}$$

While the output resistance is certainly large, a more revealing result could be obtained with a better model of the BJT. A more accurate h-parameter model of a BJT includes h_{oe} (as derived in Section 5.2). When this model is used to determine the output resistance of a simple common-emitter amplifier (see Figure 5.10b), the output resistance is given by:

$$R_o = r_o = \frac{1}{h_{oe}} = \left|\frac{V_A}{I_C}\right|. \tag{5.48}$$

The output resistance is therefore a large value which is dependent strongly on the quiescent conditions of the transistor.

As mentioned above, it is also possible to define output resistance of a common-emitter amplifier to include the collector resistor, R_c:

$$R_{ol} = R_o // R_c \approx R_c. \tag{5.49}$$

The common-emitter amplifier has been shown to have:

- moderate input resistance,
- high output resistance,
- high current gain, and
- moderate to high voltage gain, depending on the presence and size of any resistance connected to the collector terminal.

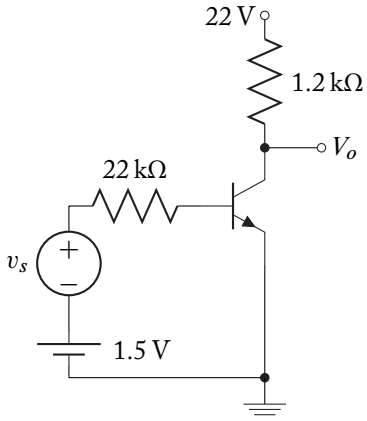
A Summary of the common-emitter amplifier performance characteristics is found in Subsection 5.3.4.

Example 5.5
Given a Silicon *npn* BJT with parameters:

$$\beta_F = 150 \qquad V_A = 350\,\text{V},$$

operating in the given circuit at room temperature.

Determine the amplifier small-signal performance characteristics.



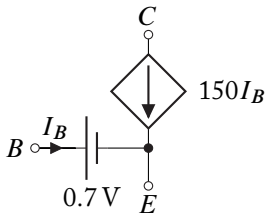
Solution:

The modeling process for transistor circuit performance was described in Section 5.2 to contain the following steps:

1. Model the BJT with an appropriate DC model.
2. Determine the circuit quiescent (DC) conditions—verify BJT active region.
3. Determine the BJT AC model parameters from the quiescent conditions.
4. Create an AC equivalent circuit.

5. Determine the circuit AC performance by:
   (a) replacing the BJT by its AC model, or
   (b) using previously derived results for the circuit topology.
6. Add the results of the DC and AC analysis to obtain total circuit performance.

Step #1 Model the BJT with an appropriate DC model. Hopefully, the BJT will be found to be in the forward-active region so that the circuit can operate as an amplifier. The DC forward-active model of the BJT is derived in Section 3.4 (Book 1), and shown below. The appropriate transistor quantities that must be used in this case are $\beta_F = 150$ and $V_\gamma = 0.7$ (Silicon BJT).



Step #2 Determine the circuit quiescent (DC) conditions—verify BJT active region.

The BJT model of step #1 replaces the BJT as shown. Quiescent conditions are then calculated. Around the base-emitter loop, Kirchhoff's Current Law yields:

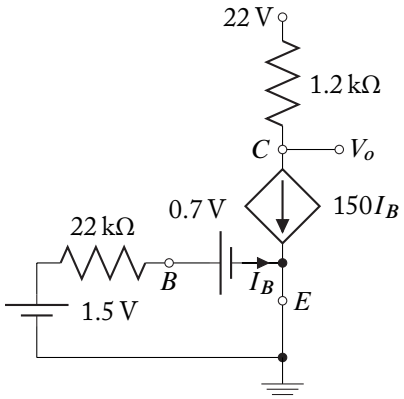
$$1.5 - 22\,\text{k}(I_B) - 0.7 = 0.$$

So that

$$I_B = 36.36\,\mu\text{A}$$

and

$$I_C = 150 I_B = 5.45\,\text{mA}.$$



Both currents are positive: only V_{CE} must be checked to see if it is larger than $V_{CE(sat)} = 0.2\,\text{V}$. Kirchhoff's Current Law applied to the collector-emitter loop yields:

$$V_{CE} = 22 - 1.2\,\text{k}(I_C) = 15.46\,\text{V}.$$

The transistor is in the forward-active region: the circuit will operate as an amplifier.

Step #3 Determine the BJT AC model parameters from the quiescent conditions.

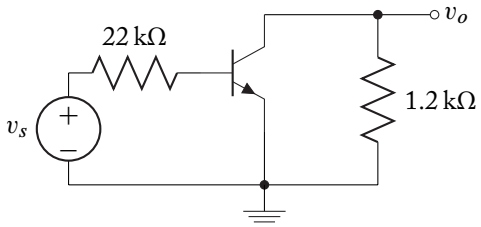
The relevant h-parameters are:

$$h_{fe} \approx \beta_F = 150 \quad h_{ie} \approx (\beta_F + 1)\frac{\eta V_t}{|I_C|} = (151)\frac{26\,\text{mV}}{|5.45\,\text{mA}|} = 720\,\Omega$$

$$h_{re} = 0 \qquad h_{oe} = \left|\frac{I_C}{V_A}\right| = \left|\frac{5.45\,\text{mA}}{350\,\text{V}}\right| = 15.6\,\mu\text{S} \approx 0.$$

Step #4 Create an AC equivalent circuit.

The DC sources are set to zero and the output voltage becomes a small-signal quantity.



Step #5 Determine the circuit AC performance by:

1. replacing the BJT by its AC model, or
2. using previously derived results for the circuit topology.

In this case, it appears easiest to use previously derived results. The input resistance at the base of the BJT is given by:

$$R_i = h_{ie} = 720\,\Omega.$$

If the input resistance is measured to the left of the 22 kΩ resistor then:

$$R_i' = 22\,\text{k}\Omega + 720\,\Omega = 22.7\,\text{k}\Omega.$$

The current gain is given by:

$$A_I = -h_{fe} = -150.$$

The voltage gain from the base of the BJT is given by:

$$A_V = \frac{-h_{fe}R_c}{h_{ie}} = \frac{-150(1.2\,\text{k})}{720} = -250.$$

The voltage gain from the source is given by:

$$A_{VS} = \frac{-h_{fe}R_c}{h_{ie} + R_s} = \frac{-150(1.2\,\text{k})}{720 + 22\,\text{k}} = -7.92.$$

The output resistance is given by:

$$R_o = \frac{1}{h_{oe}} = 64.17\,\text{k}\Omega.$$

If the collector resistance is included in the output resistance,

$$R_{ol} = R_o // R_c = \frac{(64.17\,\text{k})(1.2\,\text{k})}{64.17\,\text{k} + 1.2\,\text{k}} = 1.18\,\text{k}\Omega.$$

Step #6 is beyond the requirements of this problem, but all the data is present to add the quiescent solution to the small-signal solution for total circuit response.

5.3.1 COMMON-EMITTER AMPLIFIERS WITH NON-ZERO EMITTER RESISTANCE

Several of the characteristics of a common-emitter amplifier can be altered through the addition of a resistor connected between the emitter and ground.

It has previously been shown in Section 3.7 (Book 1) that the addition of such a resistor greatly improves bias stability due to BJT variations. The addition of an emitter resistor has the following effects on common-emitter amplifiers:

- increased input resistance,
- increased output resistance,
- decreased voltage gain, and
- unchanged current gain.

Derivation of these effects follows the process described in Section 5.2.

In order to determine the AC performance of this amplifier, the quiescent conditions must first be obtained. If the BJT is operating in the forward-active region, an AC equivalent model of the circuit can be obtained (Figure 5.12a) and the BJT can be replaced by its *h*-parameter model[11] (based on the quiescent conditions) in the AC equivalent circuit (Figure 5.12b). Circuit performance parameters can now be obtained from this equivalent circuit.

[11]The initial calculations assume that h_{oe} is small and can be ignored. Calculations to determine the effect of non-zero h_{oe} follow in Subsection 5.3.2.

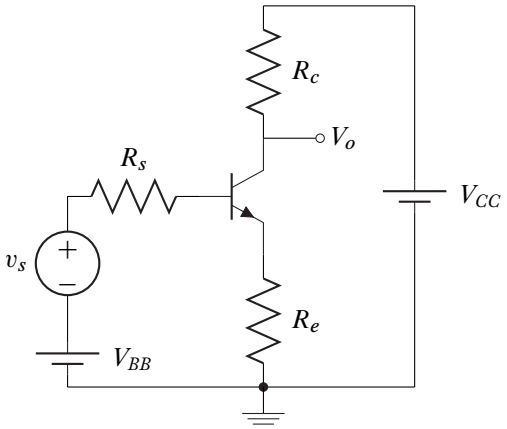


Figure 5.11: A common-emitter amplifier with an emitter resistor.

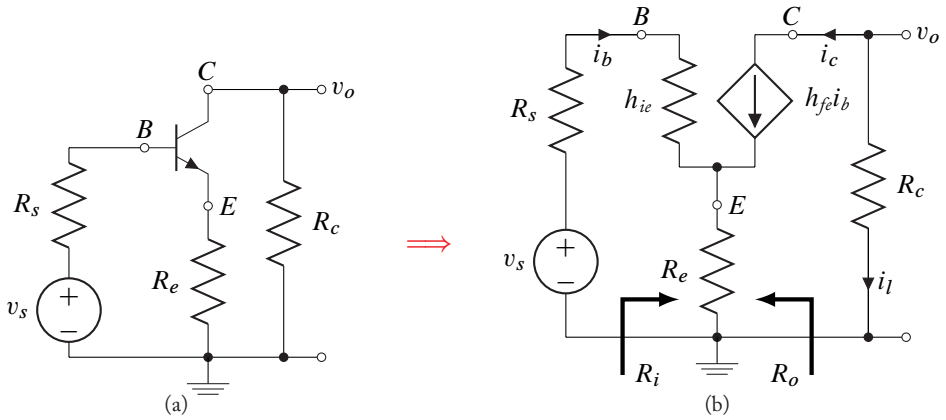


Figure 5.12: AC modeling of a common-emitter amplifier with an emitter resistor. (a) The small-signal circuit: DC sources set to zero; (b) BJT replaced by h-parameter model.

Current Gain

The current gain is defined as the ratio of load current to input current, that is:

$$A_I \equiv \frac{i_l}{i_b} = \frac{-i_c}{i_b}. \tag{5.50}$$

The ratio of collector to base current remains unchanged from the simple common-emitter amplifier. The current gain is dependent only on the BJT characteristics and independent of any

other circuit element values. Its value is given by:

$$A_I = -h_{fe}. \tag{5.51}$$

Input Resistance

The input resistance (shown in Figure 5.12b) is given by:

$$R_i \equiv \frac{v_b}{i_b} = \frac{h_{ie}i_b + R_e(i_b + h_{fe}i_b)}{i_b} = h_{ie} + (h_{fe} + 1)R_e. \tag{5.52}$$

The addition of an emitter resistor has greatly increased the input resistance of the amplifier. From the input of the BJT, the emitter resistor appears to act as a resistor in series with h_{ie} that is $(h_{fe} + 1)$ times its true value.

Voltage Gain

The voltage gain is the ratio of output voltage to input voltage. If the input voltage is again taken to be the voltage at the input to the transistor, v_b:

$$A_V \equiv \frac{v_o}{v_b}. \tag{5.53}$$

Using methods similar to those of the simple common-emitter amplifier to calculate the voltage gain yields:

$$A_V = \frac{v_o}{v_b} = \left(\frac{v_o}{i_l}\right)\left(\frac{i_l}{i_b}\right)\left(\frac{i_b}{v_b}\right), \tag{5.54}$$

or

$$A_V = (R_c)\,(A_I)\left(\frac{1}{R_i}\right) = \frac{-h_{fe}R_c}{h_{ie} + (h_{fe} + 1)R_e}. \tag{5.55}$$

For large values of h_{fe}, the external resistors dominate the expression for voltage gain. A rough approximation, which somewhat over-estimates the magnitude of the gain, is:

$$A_V \approx -\frac{R_c}{R_e}. \tag{5.56}$$

Often the voltage gain from the source to the load is of interest as well. This overall voltage gain can be defined as:

$$A_{VS} \equiv \frac{v_o}{v_s}. \tag{5.57}$$

This ratio can be directly derived from the voltage gain, A_V, and a voltage division between the source resistance, R_s, and the amplifier input resistance, R_i:

$$A_{VS} = \frac{v_o}{v_s} = \left(\frac{v_o}{v_b}\right)\left(\frac{v_b}{v_s}\right) = A_V\left(\frac{R_i}{R_i + R_s}\right), \tag{5.58}$$

or

$$A_{VS} = \left(\frac{-h_{fe}R_c}{R_i}\right)\left(\frac{R_i}{h_{ie} + (h_{fe}+1)R_e + R_s}\right) = \frac{-h_{fe}R_c}{h_{ie} + (h_{fe}+1)R_e + R_s}. \tag{5.59}$$

Output Resistance

The output resistance is defined as the Thévenin resistance at the output of the amplifier looking back into the amplifier. As in the case of the simple common-emitter amplifier, R_o is measured without considering R_c (Figure 5.12). Once again, the resistance looking into the collector of the BJT is very large, $R_o \approx \infty$.

Example 5.6

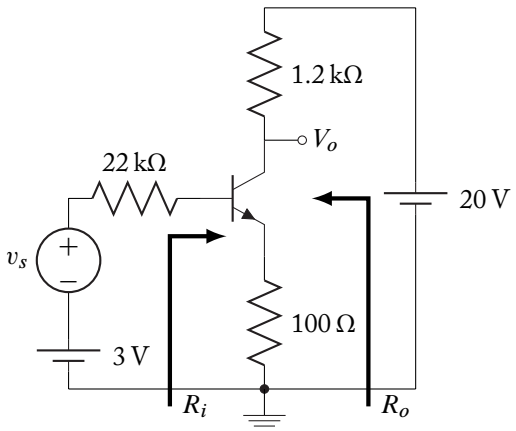
Given a Silicon *npn* BJT with parameters:

$$\beta_F = 150 \qquad V_A = 350\,\text{V},$$

operating in the given circuit at room temperature.

Determine the small-signal characteristics:

Voltage Gain, v_o/v_s
Input Resistance, R_i
Output Resistance, R_o.



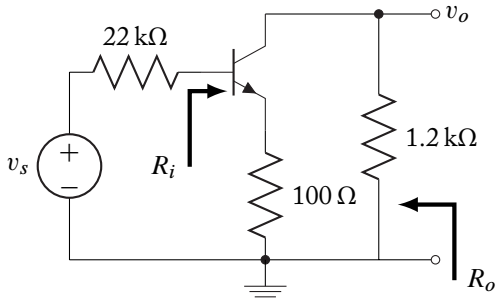
Solution:

The modeling process begins with solving for the quiescent circuit conditions. In this particular circuit, the identical transistor was placed in the same quiescent circuit in Example 5.4. There is no need to repeat identical operations to find the small-signal model of the BJT. The

results of process steps 1 through 3 were:

$$I_B = 62.0\,\mu\text{A} \quad I_C = 9.30\,\text{mA}$$
$$h_{fe} = 150 \qquad h_{ie} = 422\,\Omega \qquad r_o = 37.6\,\text{k}\Omega.$$

The next step is to create an AC equivalent circuit and insert the BJT h-parameter model into the AC equivalent circuit or use previously derived results. The general topology of a common-emitter amplifier with an emitter resistor has previous results. The AC equivalent circuit is shown below.



The voltage gain, as defined, is determined from Equation (5.59):

$$A_{VS} = \frac{-(150)(1200)}{422 + (151)(100) + 22,000} = -4.7972 \approx -4.80.$$

R_i, as shown, is given by Equation (5.52):

$$R_i = 422 + (151)(100) = 15,522 \approx 15.5\,\text{k}\Omega.$$

The output resistance, R_o, is given by the parallel combination of the output resistance of the amplifier and the collector resistor, R_c:

$$R_o \approx \infty // 1.2\,\text{k}\Omega = 1.2\,\text{k}\Omega.$$

5.3.2 THE EFFECT OF NON-ZERO h_{oe} ON COMMON-EMITTER AMPLIFIERS WITH AN EMITTER RESISTOR

As with simple common-emitter amplifiers, the effects of non-zero h_{oe} can only be seen when the collector resistance becomes large: when R_c approaches or exceeds r_o in magnitude. With simple common-emitter amplifiers, the most noticeable effect of non-zero h_{oe} is on the output resistance of the amplifier. Input resistance is unaffected, while the current and voltage gain are limited if the external collector resistance, R_c, is large. Non-zero h_{oe} in the presence of an emitter resistor effects all the common-emitter amplifier characteristics in a complex fashion.

Expressions for the input resistance, voltage gain, and current gain are obtained using the AC equivalent circuits of Figure 5.13. Figure 5.13b is obtained from the more-traditional Figure 5.13a through a source transformation on the dependent current source and r_o. Symbolic manipulations of Kirchhoff's Laws are facilitated through this well-known transformation.

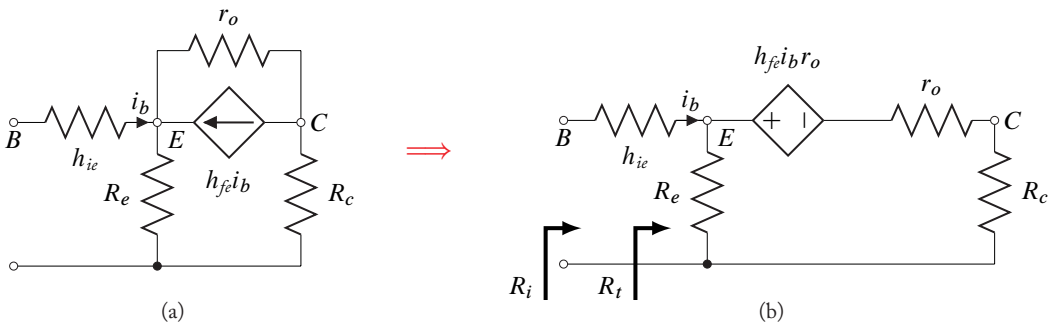


Figure 5.13: AC equivalent circuits—non-zero h_{oe}.

Input Resistance

The input resistance can be determined by first finding R_t (as shown on Figure 5.13) and then adding the resistance, h_{ie}:

$$R_i = h_{ie} + R_t. \tag{5.60}$$

In the usual Thévenin process, a voltage, v, is applied across R_e. The input current is then found to be:

$$i_b = \frac{v}{R_e} + \frac{v - h_{fe} i_b r_o}{r_o + R_c}. \tag{5.61}$$

Collecting terms yields:

$$i_b \left\{ \frac{(1 + h_{fe}) r_o}{r_o + R_c} \right\} = v \left\{ \frac{1}{R_e} + \frac{1}{r_o + R_c} \right\}. \tag{5.62}$$

Which leads to the Thévenin resistance, R_t:

$$R_t = \frac{v}{i_b} = (1 + h_{fe}) R_e \left[\frac{r_o}{r_o + R_c + R_e} \right]. \tag{5.63}$$

The desired input resistance is found using Equation (5.60):

$$R_i = h_{ie} + R_t = h_{ie} + (1 + h_{fe}) R_e \left[\frac{r_o}{r_o + R_c + R_e} \right]. \tag{5.64}$$

An interesting result of these calculations is that large values of the collector resistor, R_c, will *reduce* the value of the amplifier input resistance!

Voltage Gain

The voltage gain can be calculated as follows by continuing with the circuit of Figure 5.13 and many of the calculations used in determining the input resistance. The output voltage for this circuit is taken across the collector resistor, R_c. It can be obtained through a simple voltage division from the voltage, v, (taken across R_e):

$$v_o = \frac{R_c}{R_c + r_o}\left[v - h_{fe} i_b r_o\right], \tag{5.65}$$

where, including the presence of h_{ie} in Figure 5.13,

$$v = v_s\left[\frac{R_t}{h_{ie} + R_t}\right] \quad \text{and} \quad i_b = \frac{v_s}{h_{ie} + R_t}. \tag{5.66}$$

Substitution of these two expressions into Equation (5.65) leads directly to the voltage gain:

$$A_V = \frac{v}{v_s} = -\frac{h_{fe}(R_c // r_o)}{R_i} + \frac{R_c}{R_c + r_o}\frac{R_t}{R_i} \approx -\frac{h_{fe}(R_c // r_o)}{R_i}. \tag{5.67}$$

For the special case of significantly large R_e,

$$R_e \gg \frac{\eta V_t}{|I_c|},$$

the numerator and denominator of this expression have approximately the same dependence on the relationship of R_c and r_o. The voltage gain *for this special case of large* R_e is *approximately independent of* r_o and unchanged from the expression of Equation (5.55).

$$A_V \approx \frac{-h_{fe} R_c}{h_{ie} + (h_{fe} + 1)R_e}. \tag{5.68}$$

Current Gain

The current gain can be calculated using Equations (5.66) and the two expressions:

$$i_o = \frac{v_o}{R_c} \qquad \text{and} \qquad v = i_b R_t, \tag{5.69}$$

and:

$$i_o = \frac{v_o}{R_c} = \frac{1}{R_c + r_o}(i_b R_t - h_{fe} i_b r_o). \tag{5.70}$$

From which the current gain is calculated:

$$A_I = \frac{i_o}{i_b} = -\frac{h_{fe} r_o}{r_o + R_c} + \frac{R_t}{r_o + R_c} \approx -\frac{h_{fe} r_o}{r_o + R_c}. \tag{5.71}$$

Basically, the output current is divided between the collector resistor and r_o. It decreases as the collector resistance increases in magnitude.

Output Resistance

Calculations to determine output resistance including the effect of the BJT output resistance, r_o, are based on an AC equivalent circuit with a more complete h-parameter model of the BJT as shown in Figure 5.14.

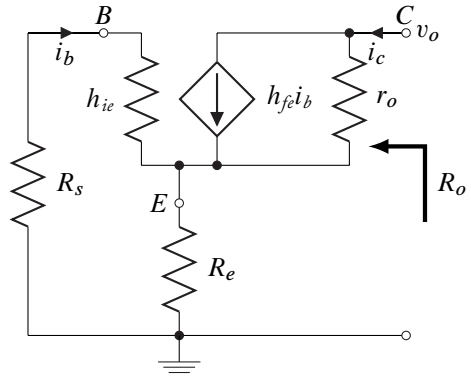


Figure 5.14: Circuit for calculation of output resistance.

If a current, i, is applied to the collector terminal, the base current can be found through a current division:

$$i_b = \frac{-R_e}{R_e + h_{ie} + R_s}. \tag{5.72}$$

The voltage that appears at the output terminals is then given by:

$$v = \{R_e // (R_s + h_{ie})\} i + r_o \left(i - h_{fe} i_b\right) \tag{5.73}$$

or, including the relationship between i and i_b:

$$v = \{R_e // (R_s + h_{ie})\} i + \left\{r_o + \frac{h_{fe} R_e r_o}{R_e + h_{ie} + R_s}\right\} i. \tag{5.74}$$

Simple division leads to the expression for the output resistance:

$$R_o = \frac{v}{i} = \{R_e // (R_s + h_{ie})\} + r_o \left\{1 + \frac{h_{fe} R_e}{R_e + h_{ie} + R_s}\right\}. \tag{5.75}$$

This is a *very* large resistance: the addition of an emitter resistor has significantly increased the output resistance over the simple common-emitter amplifier (the increase is by a factor on the order of $\{h_{fe} + 1\}$). The infinite output resistance approximation, $R_o \approx \infty$, is therefore valid over a greater range of load resistance, R_c, than in the simple common-emitter amplifier.

5.3.3 COUPLING AND BYPASS CAPACITORS

Often the demands of properly biasing a BJT into the forward-active region and applying an AC signal to the input create conflicting circuit topology requirements. It is not always possible to put the AC input in series with a DC biasing voltage as has been previously described. In addition, the need for high voltage gain and good bias stability creates a design requirement conflict in the magnitude of the emitter resistor, R_e. One *possible* design alternative that can resolve these conflicts involves the use of capacitors to couple the AC signal into the amplifier and/or to bypass the emitter resistor.

If an AC signal is imposed upon a capacitor, the complex impedance of the capacitor is given by:

$$z_C = \frac{1}{j\omega C},$$

where

$C =$ the capacitance of the capacitor in farads (F)
$\omega =$ the frequency of the sinusoidal signal in rad/sec.

At DC ($\omega = 0$), the capacitor has infinite impedance: a capacitor blocks DC signals. If either the frequency or the capacitance is large, the impedance approaches zero or becomes relatively small compared to adjacent circuit resistances. For purposes of demonstration, assume that a band of frequencies exist for which the impedance of all discrete capacitors in a circuit will be essentially zero. This band of frequencies is called the *midband frequency region*[12] of a circuit. If the AC input signals to a circuit are within the midband frequency region of the circuit, each discrete capacitor will appear to be the equivalent of a short circuit. Each capacitor will, however, appear to be the equivalent of an open circuit to the bias (DC) circuitry.[13]

In the presence of coupling and/or bypass capacitors, the modeling of amplifier circuit performance is slightly altered. In determining quiescent conditions, each capacitor is replaced by an open circuit in addition to replacing the BJT with an appropriate model. The AC equivalent circuit is drawn with each capacitors replaced by a short.

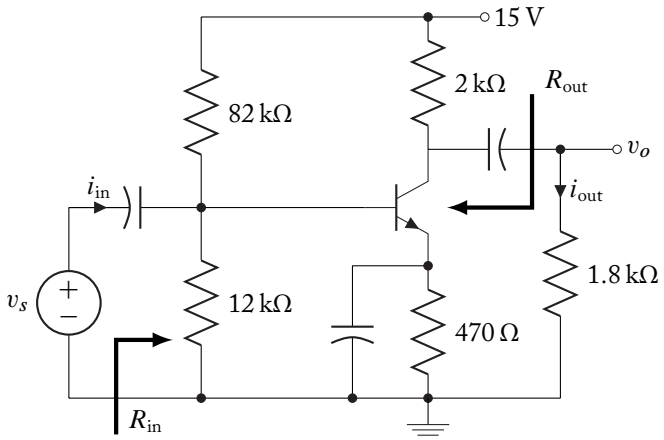
Example 5.7
A Silicon BJT with parameters:

$$\beta_F = 150 \quad \text{and} \quad V_A = 350,$$

[12]Often called the *midband region.*
[13]The transition as frequency increases between an apparent open circuit and an apparent short circuit is beyond these early discussions. It is extensively covered in Section III—Frequency Dependence.

is placed in the amplifier shown. Assume the amplifier is operating in its midband frequency range, and determine the following circuit performance parameters:

$$A_V = \frac{v_o}{v_s}, \quad A_I = \frac{i_{out}}{i_{in}},$$
$$R_{in}, \quad \text{and} \quad R_{out}.$$



Solution:

The quiescent point of the BJT must be found first to ensure that it is in the forward-active region and to find its h-parameters. For DC operation, all capacitors appear as open circuits. The DC equivalent circuit, after replacing the base circuit with its Thévenin equivalent, is shown below:

The base and collector currents are:

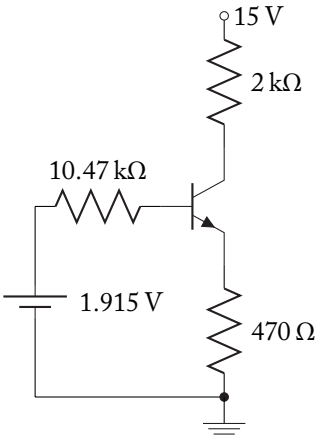
$$I_B = \frac{1.915 - 0.7}{10.47\,\text{k} + 151(470)} = 14.92\,\mu\text{A},$$

and

$$I_C = 150 I_B = 2.238\,\text{mA}.$$

V_{CE} must be checked to verify that the BJT is in the forward-active region.

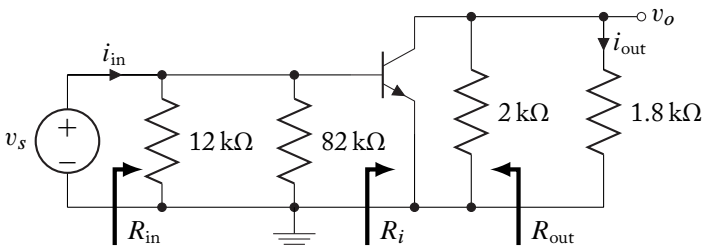
$$V_{CE} = 15 - I_C(2\,\text{k}) - \frac{151}{150} I_C(470) = 9.47\,\text{V} \geq 0.2\,\text{V}.$$



Now that the forward-active region is verified, the BJT h-parameters can be determined:

$$h_{fe} = 150, \quad h_{ie} = 151\frac{\eta V_t}{|I_C|} = 1.755\,\text{k}\Omega, \quad \text{and} \quad \frac{1}{h_{oe}} = \left|\frac{V_A}{I_C}\right| = 156.4\,\text{k}\Omega.$$

An AC equivalent circuit can now be determined. All DC sources are set to zero and, since the circuit is in its midband frequency range, all capacitors are replaced by short circuits: the 470 Ω resistor is totally eliminated from the circuit. The AC equivalent circuit leads to the determination of amplifier performance characteristics.



$$A_V = -\frac{h_{fe}R_c}{h_{ie}} = -\frac{150(2\,\text{k}//1.8\,\text{k})}{1.755\,\text{k}} = -81.0$$
$$R_{in} = 82\,\text{k}//12\,\text{k}//R_i = 10.47\,\text{k}//h_{ie} = 1.50\,\text{k}\Omega$$
$$R_{out} = 2\,\text{k}//r_o = 1.98\,\text{k} \approx 2.0\,\text{k}\Omega$$
$$A_I = \frac{i_{out}}{i_{in}} = \left(\frac{i_{out}}{v_o}\right)\left(\frac{v_o}{v_s}\right)\left(\frac{v_s}{i_{in}}\right) = \left(\frac{1}{1.8\,\text{k}}\right)(-81.0)(1.50\,\text{k}) = -67.5.$$

5.3.4 SUMMARY OF COMMON-EMITTER AMPLIFIER PROPERTIES

A summary of common-emitter amplifier performance characteristics, as derived in this section, is given in Table 5.3.

Table 5.3: Common-emitter amplifier characteristics

	CE	CE $+R_e$
A_I	$-h_{fe}$	$-h_{fe}$
R_i	h_{ie}	$h_{ie} + (h_{fe} + 1)R_e$
A_V	$\dfrac{-h_{fe}R_c}{h_{ie}}$	$\dfrac{-h_{fe}R_c}{h_{ie} + (h_{fe} + 1)R_e}$
R_o	$\dfrac{1}{h_{oe}} \approx \infty$	$\approx \infty$

5.4 COMMON-COLLECTOR AMPLIFIERS

Common-collector amplifiers have the following general circuit topology:

- the input signal enters the BJT at the base,
- the output signal exits the BJT at the emitter, and
- the collector is connected to a constant voltage, often the ground (common) terminal, sometimes with an intervening resistor.

A simple common-collector amplifier is shown in Figure 5.15. The collector resistor, R_c, is unnecessary in many applications, it is shown here for generality. The quiescent point of the BJT must be set with the circuitry external to the transistor so that it is in the forward-active region. The values of the resistors, R_c and R_b, and the DC voltage sources, V_{CC} and V_{BB}, have therefore been chosen so that the BJT is in the forward-active region and the circuit will operate as an amplifier.

Once the circuit quiescent conditions have been calculated and it has been determined that the BJT is in the forward-active region of operation, the significant h-parameters are calculated to form the small-signal model of the transistor:

$$\begin{aligned} h_{fe} &= \beta_F \qquad h_{oe} = \frac{I_C}{V_A} \approx 0. \\ h_{ie} &= (\beta_F + 1)\left|\frac{\eta V_t}{I_C}\right|. \end{aligned} \tag{5.76}$$

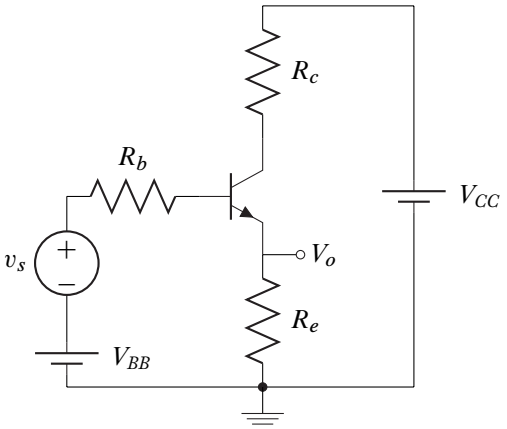


Figure 5.15: A typical common-collector amplifier.

The small-signal circuit performance can now be calculated. Total circuit performance is the sum of quiescent and small-signal performance. The process of AC modeling of the circuit and replacing the BJT with an appropriate AC model, applied to Figure 5.15, is shown in Figure 5.16.

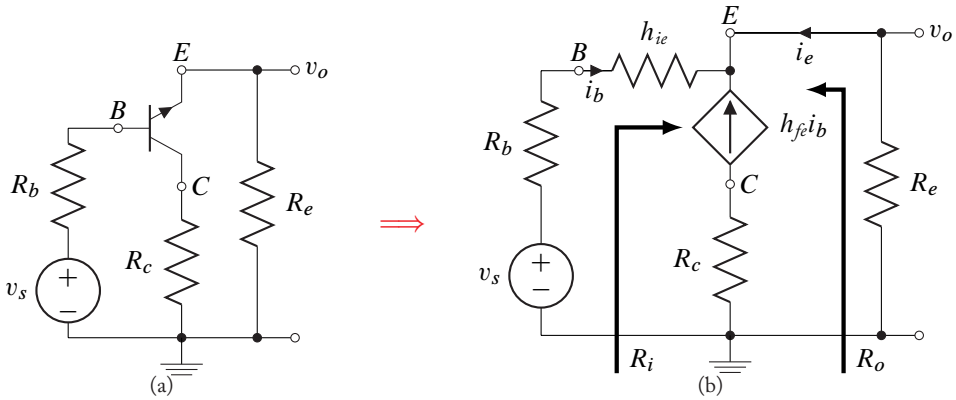


Figure 5.16: AC modeling of a common-collector amplifier. (a) The small-Signal circuit: DC sources set to zero; (b) BJT replaced by h-parameter model.

The small-signal performance can be obtained from analysis of the circuit of Figure 5.16b. Definitions for these quantities often vary due to differing definition of the exact location of the point of measurement. Care must always be taken to *ensure that measurement points are clearly understood before any analysis begins*. Many similarities exist between the circuit topologies of a

common-collector amplifier and a common-emitter amplifier with an emitter resistor: those similarities will be utilized in calculating common-collector amplifier performance characteristics.

Current Gain

For this simple transistor amplifier, the current gain is defined as the ratio of load current to input current, that is:

$$A_I \equiv \frac{i_l}{i_b} = \frac{-i_e}{i_b}. \tag{5.77}$$

From the circuit of Figure 5.16b, it can be determined that the emitter and base currents are related through the dependent current source by the constant $h_{fe} + 1$. The current gain is dependent only on the BJT characteristics and independent of any other circuit element values. Its value is given by:

$$A_I = h_{fe} + 1. \tag{5.78}$$

Input Resistance

The input resistance (shown in Figure 5.16b) is given by:

$$R_i \equiv \frac{v_b}{i_b} = \frac{h_{ie} i_b + R_e(i_b + h_{fe} i_b)}{i_b} = h_{ie} + (h_{fe} + 1) R_e. \tag{5.79}$$

This result is identical to that for a common-emitter amplifier with an emitter resistor. The input resistance to a common-collector amplifier is large for typical values of the load resistance, R_e.

Voltage Gain

The voltage gain is the ratio of output voltage to input voltage. If the input voltage is again taken to be the voltage at the input to the transistor, v_b:

$$A_V \equiv \frac{v_o}{v_b}. \tag{5.80}$$

Using previously introduced methods to calculate the voltage gain yields:

$$A_V = \frac{v_o}{v_b} = \left(\frac{v_o}{i_l}\right)\left(\frac{i_l}{i_b}\right)\left(\frac{i_b}{v_b}\right), \tag{5.81}$$

or, replacing each term with its equivalent expression:

$$A_V = (R_e)(A_I)\left(\frac{1}{R_i}\right) = \frac{(h_{fe} + 1) R_e}{h_{ie} + (h_{fe} + 1) R_e}. \tag{5.82}$$

Equation (5.82) is somewhat less than unity. A form of the voltage gain expression that shows this approximation is:

$$A_V = 1 - \frac{h_{ie}}{h_{ie} + (h_{fe} + 1) R_e} = 1 - \frac{h_{ie}}{R_i} \approx 1. \tag{5.83}$$

Often the voltage gain from the source to the load is of interest as well. This overall voltage gain can be defined as:

$$A_{VS} \equiv \frac{v_o}{v_s}. \tag{5.84}$$

This ratio can be directly derived from the voltage gain, A_V, and a voltage division between the source resistance, R_s, and the amplifier input resistance, R_i:

$$A_{VS} = \frac{v_o}{v_s} = \left(\frac{v_o}{v_b}\right)\left(\frac{v_b}{v_s}\right) = A_V\left(\frac{R_i}{R_i + R_b}\right). \tag{5.85}$$

Appropriate substitutions lead to:

$$A_{VS} = 1 - \frac{h_{ie} + R_b}{R_i + R_b}. \tag{5.86}$$

Output Resistance

The output resistance is defined as the Thévenin resistance at the output of the amplifier looking back into the amplifier. The circuit of Figure 5.17 defines the necessary topology and circuit variables for output resistance calculations.

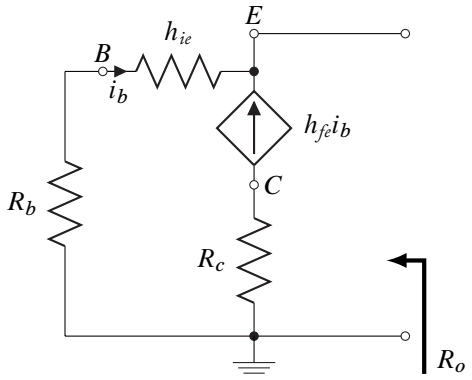


Figure 5.17: Common-collector output resistance AC equivalent circuit.

If a voltage, v, is applied to the output terminals, the base current is found to be:

$$i_b = \frac{-v}{R_b + h_{ie}}. \tag{5.87}$$

The total current flowing into the emitter of the BJT is given by:

$$i = -i_b - h_{fe}i_b. \tag{5.88}$$

From which the output resistance is calculated:

$$R_o = \frac{v}{i} = \frac{R_b + h_{ie}}{h_{fe} + 1}. \tag{5.89}$$

The output resistance for a common-collector amplifier is typically small.

The common-collector amplifier has been shown to have:

- high input resistance,
- low output resistance,
- high current gain, and
- low voltage gain.

A summary of common-collector performance characteristics, as derived in this section, is given in Table 5.4.

Table 5.4: Common-collector amplifier characteristics[14]

A_I	$h_{fe} + 1$
R_i	$h_{ie} + (h_{fe} + 1)R_e$
A_V	$1 - \frac{h_{ie}}{R_i}$
R_o	$\frac{R_b + h_{ie}}{h_{fe} + 1}$

Example 5.8

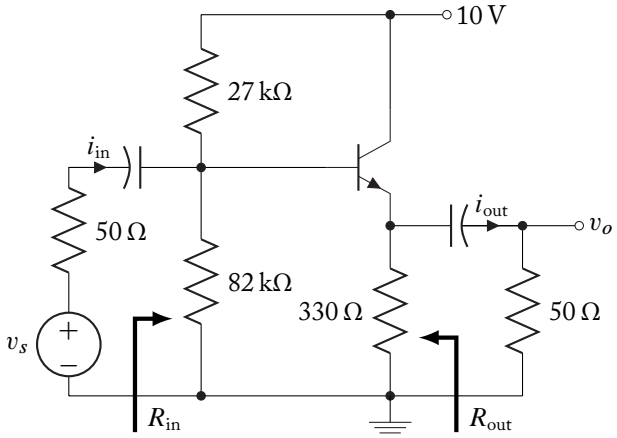
A Silicon BJT with parameters:

$$\beta_F = 100 \quad \text{and} \quad V_A = 250\,\text{V},$$

is placed in the amplifier shown. Assuming the amplifier is operating in its midband frequency range, determine the following circuit performance parameters:

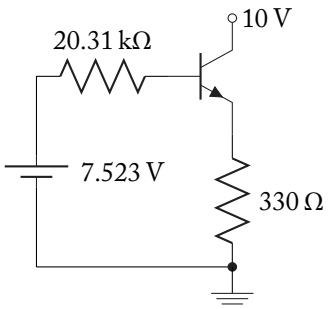
$$A_V = \frac{v_o}{v_s},\ A_I = \frac{i_{out}}{i_{in}},\ R_{in} \text{ and } R_{out}.$$

[14]These characteristics are based on approximations assuming that the BJT output resistance, r_o, is much larger than the sum of the total resistance connected to the collector and emitter terminals of the transistor. Large resistances necessitate the use of the expressions derived in Subsection 5.4.1.



Solution:

The quiescent point of the BJT must be found first to ensure that it is in the forward-active region and to find its h-parameters. For DC operation, all capacitors appear as open circuits. The DC equivalent circuit, after replacing the base circuit with its Thévenin equivalent, is shown below:



The base and collector currents are:

$$I_B = \frac{7.523 - 0.7}{20.31\,\text{k} + 101(330)} = 127.2\,\mu\text{A},$$

and

$$I_C = 100 I_B = 12.72\,\text{mA}.$$

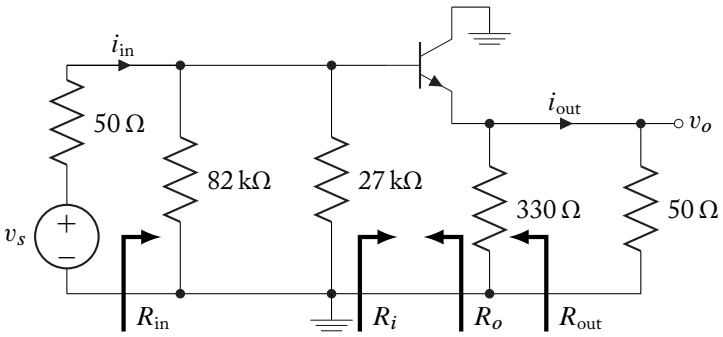
V_{CE} must be checked to verify that the BJT is in the forward-active region.

$$V_{CE} = 10 - \frac{101}{100} I_C (330) = 5.76\,\text{V} \geq 0.2\,\text{V}.$$

The BJT h-parameters can now be determined:

$$h_{fe} = 100,\ h_{ie} = 101\frac{\eta V_t}{|I_C|} \approx 210\,\Omega,\ \text{and}\ \frac{1}{h_{oe}} = \left|\frac{V_A}{I_C}\right| = 19.65\,\text{k}\Omega.$$

An AC equivalent circuit can now be determined. All DC sources are set to zero and, since the circuit is in its midband frequency range, all capacitors are replaced by short circuits. The AC equivalent circuit leads to the determination of amplifier performance characteristics. Care must be taken concerning parameter definitions.



$$\begin{aligned}
R_i &= h_{ie} + (h_{fe} + 1)R_e \\
&= 210 + (101)(330//50) = 4.596\,\text{k}\Omega \\
R_{in} &= 82\,\text{k}\Omega//27\,\text{k}\Omega//R_i = 3.75\,\text{k}\Omega \\
A_v &= \frac{v_o}{v_s} = \left(\frac{v_o}{v_b}\right)\left(\frac{v_b}{v_s}\right) = \left(1 - \frac{h_{ie}}{R_i}\right)\left(\frac{R_{in}}{R_{in} + 50}\right) = \left(1 - \frac{210}{4596}\right)\left(\frac{3750}{3800}\right) = 0.942 \\
R_o &= \frac{R_b + h_{ie}}{h_{fe} + 1} = \frac{50//82\,\text{k}//27\,\text{k} + 210}{101} = 2.573\ \Omega \\
R_{out} &= R_o//330 = 2.55\,\Omega \\
A_I &= \frac{i_{out}}{i_{in}} = \left(\frac{i_b}{i_{in}}\right)\left(\frac{i_o}{i_b}\right)\left(\frac{i_{out}}{i_o}\right) = \left(\frac{82\,\text{k}//27\,\text{k}}{82\,\text{k}//27\,\text{k} + 3.75\,\text{k}}\right)(101)\left(\frac{330}{330 + 50}\right) = 74.0.
\end{aligned}$$

5.4.1 THE EFFECT OF NON-ZERO h_{oe} ON COMMON-COLLECTOR AMPLIFIERS

The basic circuit topology of a common-collector amplifier is essentially the same as a common-emitter amplifier with an emitter resistor. The only significant difference is the location of the output. Many of the calculations necessary to obtain amplifier performance characteristics can be drawn from those performed in Section 5.3.2. Figure 5.18 serves as a reference for amplifier performance calculations.

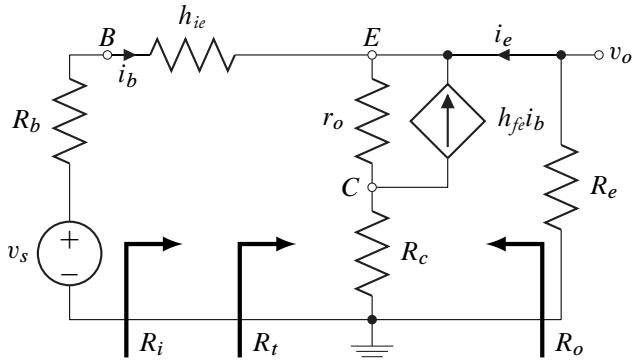


Figure 5.18: AC equivalent circuit—common-collector amplifier.

Current Gain

The current gain is defined as the ratio of load to base current:

$$A_I = \frac{-i_e}{i_b}. \tag{5.90}$$

In the circuit diagram of Figure 5.18 it can be seen that:

$$i_b = \frac{v_o}{R_t} \quad \text{and} \quad -i_e = \frac{v_o}{R_e}. \tag{5.91}$$

The quantity R_t is measured here in the identical fashion as with a common-emitter amplifier with an emitter resistor. Using the results obtained in Section 5.3 (Equation (5.63)), the current gain becomes:

$$A_I = \frac{R_t}{R_e} = \frac{(h_{fe}+1)R_e\left[\dfrac{r_o}{r_o+R_c+R_e}\right]}{R_e}, \tag{5.92}$$

which can be simplified to become:

$$A_I = \frac{(h_{fe}+1)r_o}{r_o+R_c+R_e}. \tag{5.93}$$

Current gain is reduced by the presence of non-zero h_{oe}.

Input Resistance

The input resistance of a common-collector amplifier is identical to the input resistance of a common-emitter amplifier with an emitter resistor:

$$R_i = h_{ie} + (h_{fe}+1)R_e\left[\frac{r_o}{r_o+R_c+R_e}\right]. \tag{5.94}$$

As in the common-emitter case, the input resistance is reduced.

Voltage Gain

The voltage gain can be obtained as a voltage division between h_{ie} and R_t:

$$A_V = \frac{v_o}{v_b} = \frac{R_t}{h_{ie} + R_t} = 1 - \frac{h_{ie}}{R_i}, \tag{5.95}$$

which is the same equation as (5.83) except for the definition of R_i. Here, R_i is given by Equation (5.94): the slight decrease in R_i due non-zero h_{oe} will also very slightly reduce the gain.

Output Resistance

The output resistance is best calculated by setting the input source to zero and performing a source transformation on the dependent current source in Figure 5.18. In order to simplify the diagram, the BJT output resistance, r_o has been combined with the collector resistor, R_c, into a single resistance, $R_c + r_o$.

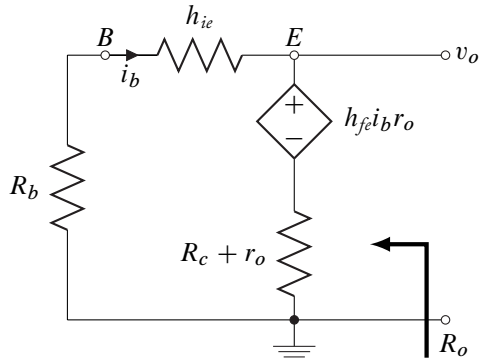


Figure 5.19: AC equivalent circuit for output resistance calculation.

If a voltage, v, is applied across the output terminals, the total current flowing into the terminal is given by:

$$i = -i_b + \frac{v - h_{fe}i_br_o}{r_o + R_c}, \tag{5.96}$$

where,

$$i_b = -\frac{v}{h_{ie} + R_b}. \tag{5.97}$$

Substitution of Equation (5.97) into Equation (5.96) leads to:

$$R_o = \frac{v}{i} = \frac{h_{ie}}{1 + \dfrac{1 + h_{fe} r_o}{r_o + R_c}} \approx \frac{h_{ie}}{1 + h_{fe}\left(\dfrac{r_o}{r_o + R_c}\right)}. \tag{5.98}$$

Non-zero h_{oe} will slightly increase the output resistance.

5.5 COMMON-BASE AMPLIFIERS

Common-base amplifiers have the following general circuit topology:

- the input signal enters the BJT at the emitter,
- the output signal exits the BJT at the collector, and
- the base is connected to a constant voltage, often the ground (common) terminal, sometimes with an intervening resistor.

A simple common-base amplifier is shown in Figure 5.20. The quiescent point of the BJT must be set with the circuitry external to the transistor so that it is in the forward-active region. The values of the resistors, R_c, the base resistors, R_{b1} and R_{b2}, and the DC voltage sources, V_{CC} and V_{BB}, have therefore been chosen so that the BJT is in the forward-active region and the circuit will operate as an amplifier.

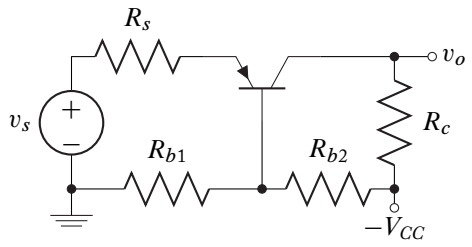


Figure 5.20: A typical common-base amplifier.

The circuit quiescent conditions must be determined to ensure that the BJT is in the forward-active region of operation. The significant h-parameters are then calculated to form the small-signal model of the transistor:

$$h_{fe} = \beta_F \qquad h_{oe} = \frac{I_C}{V_A} \approx 0. \tag{5.99}$$
$$h_{ie} = (\beta_F + 1)\left|\frac{\eta V_t}{I_C}\right|.$$

The small-signal circuit performance can now be calculated. Total circuit performance is, as usual, the sum of quiescent and small-signal performance. The process of AC modeling of the circuit and replacing the BJT with an appropriate AC model, applied to Figure 5.20, is shown in Figure 5.21. In order to simplify calculations, the base resistors have been combined as a parallel combination:

$$R_b = R_{b1} // R_{b2}. \tag{5.100}$$

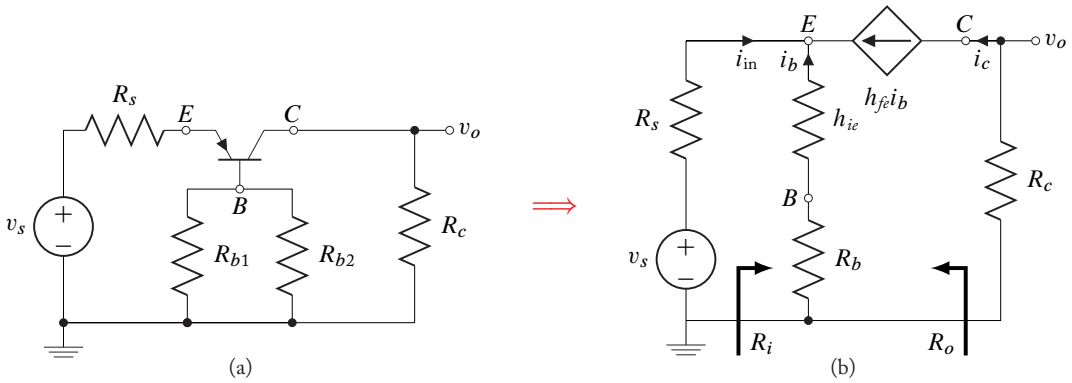


Figure 5.21: AC modeling of a common-base amplifier. (a) The small-signal circuit: DC sources set to zero. (b) BJT replaced by *h*-parameter model.

The small-signal performance can be obtained from analysis of the circuit of Figure 5.21b. Definitions for these quantities often vary due to differing definition of the exact location of the point of measurement. Care must always be taken to *ensure that measurement points are clearly understood before any analysis begins*. A few similarities exist between the circuit topologies of a common-base amplifier and the other amplifier types previously discussed: those similarities will be utilized in calculating performance characteristics.

Current Gain

For this simple transistor amplifier, the current gain is defined as the ratio of load current to input current, that is:

$$A_I \equiv \frac{i_l}{i_{in}} = \frac{-i_c}{i_e}. \tag{5.101}$$

This current ratio for a BJT in the forward-active region is well-known:

$$A_I = \frac{h_{fe}}{h_{fe} + 1}. \tag{5.102}$$

This gain is very nearly unity.

Input Resistance

The input resistance is defined as:

$$R_i = \frac{v_e}{i_{in}} = \left(\frac{v_e}{i_b}\right)\left(\frac{i_b}{i_{in}}\right) = (R_b + h_{ie})\left(\frac{1}{h_{fe}+1}\right). \tag{5.103}$$

Common-base amplifiers have low input resistance.

Voltage Gain

The voltage gain is the ratio of output voltage to input voltage. If the input voltage is again taken to be the voltage at the input to the transistor, v_e:

$$A_V \equiv \frac{v_o}{v_e}. \tag{5.104}$$

Using previously introduced methods to calculate the voltage gain yields:

$$A_V = \frac{v_o}{v_e} = \left(\frac{v_o}{i_l}\right)\left(\frac{i_l}{i_{in}}\right)\left(\frac{i_{in}}{v_e}\right), \tag{5.105}$$

or, after replacing each term with its value,

$$A_V = (R_c)\,(A_I)\left(\frac{1}{R_i}\right) = \frac{h_{fe}R_c}{h_{ie}+R_b}. \tag{5.106}$$

The voltage gain can be large and is non-inverting.

Output Resistance

The output resistance is defined as the Thévenin resistance at the output of the amplifier looking back into the amplifier. The circuit topology for this operation is the same as for the common-emitter amplifier with an emitter resistor (with the names of the resistors changed). The results are the same:

$$R_o \approx \infty, \tag{5.107}$$

a very large value.

The common-base amplifier has been shown to have:

- low input resistance,
- high output resistance,
- low gain, and
- moderate to high voltage gain.

Table 5.5: Summary of common-base amplifier performance characteristics[15]

A_I	$\dfrac{h_{fe}}{h_{fe}+1}$
R_i	$\dfrac{h_{ie}+R_b}{h_{fe}+1}$
A_V	$\dfrac{h_{fe}R_c}{h_{ie}+R_b}$
R_o	$\approx \infty$

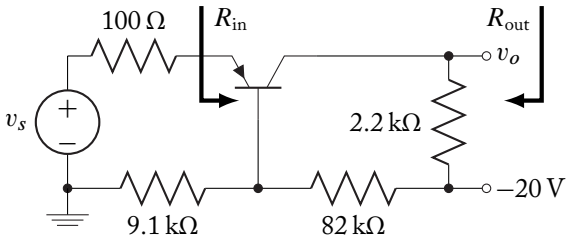
A summary of common-base performance characteristics, as derived in this section, is given in Table 5.5. Increased voltage gain and decreased input resistance can be obtained with a bypass capacitor from the BJT base terminal to ground thereby making $R_b = 0$ in the AC sense.

Example 5.9
A Silicon BJT with parameters:

$$\beta_F = 120, \qquad V_A = -200\,\text{V},$$

is placed in the amplifier shown. Determine the following circuit performance parameters:

$$A_V = \frac{v_o}{v_s},\ R_{in},\ \text{and}\ R_{out}.$$



Solution:

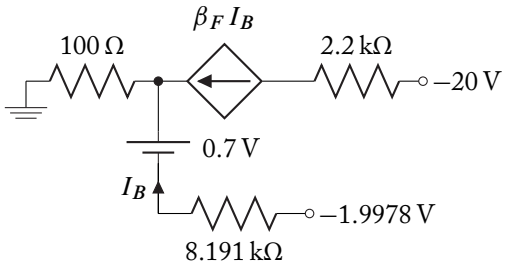
The DC equivalent circuit is shown below (a Thévenin equivalent of the base biasing circuit was made). The quiescent conditions can be calculated beginning with the base current. Around the base-emitter loop, Kirchhoff's Voltage Law yields:

$$121 I_B(100) - 0.7 + I_B(8191) + 1.998 = 0$$

[15]These characteristics are based on approximations assuming that the BJT output resistance, r_o, is much larger than the sum of the total resistance connected to the collector and emitter terminals of the transistor. Large resistances necessitate the use of the expressions derived in Subsection 5.5.1.

or,

$$I_B = -63.96\,\mu\text{A} \quad I_C = \beta_F I_B = -7.675\,\text{mA}.$$



The collector-emitter voltage is:

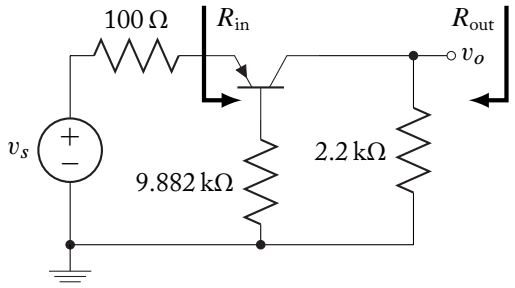
$$V_{CE} = -20 - (121 I_B)(100) - (I_C)(2200) = -2.341\,\text{V}.$$

The constraints for a *pnp* BJT in the forward-active region are met.

The *h*-parameters for the *pnp* BJT are obtained in the same manner as *npn* BJT parameters. At this quiescent point they are given by:

$$h_{fe} = 120, \quad h_{ie} = 121\frac{\eta V_t}{|I_C|} \approx 410\,\Omega, \quad \text{and} \quad \frac{1}{h_{oe}} = \left|\frac{V_A}{I_C}\right| = 26.06\,\text{k}\Omega.$$

The AC equivalent circuit is shown below. The circuit performance parameters can be calculated as:



$$R_{in} = \frac{h_{ie} + R_b}{h_{fe} + 1} = \frac{410 + 9191}{121} = 71.1\,\Omega$$

$$R_{out} = 2.2\,\text{k}\Omega$$

$$A_V = \frac{v_o}{v_s} = \left(\frac{v_o}{v_e}\right)\left(\frac{v_e}{v_s}\right) = \left(\frac{h_{fe} R_c}{h_{ie} + R_b}\right)\left(\frac{R_{in}}{R_{in} + 100}\right)$$

$$= \left(\frac{(120)(2200)}{410 + 8191}\right)\left(\frac{71.1}{71.1 + 100}\right) = 12.76.$$

5.5.1 THE EFFECT OF NON-ZERO h_{oe} ON COMMON-BASE AMPLIFIERS

Non-zero h_{oe} is modeled by altering the circuit of Figure 5.21b to include the output resistance, r_o, of the BJT. After a source transformation is performed on the dependent current source, the AC equivalent circuit becomes the circuit shown in Figure 5.22.

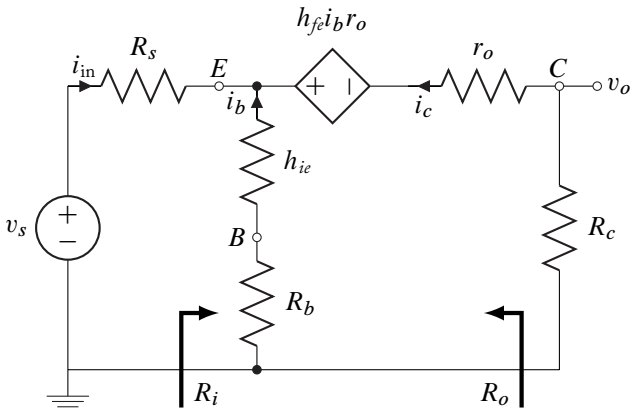


Figure 5.22: Common-base amplifier AC equivalent circuit including r_o.

Input Resistance

If a voltage, v_e, is applied to the emitter of the amplifier (assuming the source and source resistor are removed), the input current is given by:

$$i_{in} = \frac{v_e}{h_{ie} + R_b} + \frac{v_e - h_{fe} i_b r_o}{r_o + R_c}, \tag{5.108}$$

where

$$i_b = \frac{-v_e}{h_{ie} + R_b}. \tag{5.109}$$

Substituting (5.109) into (5.108) yields:

$$i_{in} = \frac{v_e}{h_{ie} + R_b} + \frac{v_e}{r_o + R_c}\left(1 + \frac{h_{fe} r_o}{h_{ie} + R_b}\right). \tag{5.110}$$

The input resistance can now be determined as:

$$R_i = \frac{v_e}{i_{in}} = \frac{h_{ie} + R_b}{1 + \left(\dfrac{h_{ie} + R_b + h_{fe} r_o}{r_o + R_c}\right)}. \tag{5.111}$$

In typical common-base amplifiers, R_b is not a large resistance. It is therefore reasonable to assume that:

$$h_{ie} + R_b \ll h_{fe} r_o. \tag{5.112}$$

Under that assumption, the input resistance expression reduces to:

$$R_i \approx \frac{h_{ie} + R_b}{1 + h_{fe}\left(\dfrac{r_o}{r_o + R_c}\right)}. \tag{5.113}$$

The presence of non-zero h_{oe} increases the input resistance.

Current Gain

The current gain is defined as the output current divided by the input current:

$$A_I = \frac{-i_c}{i_{in}}. \tag{5.114}$$

The output current was expressed as a component of Equation (5.110):

$$-i_c = \frac{v_e}{r_o + R_c}\left(1 + \frac{h_{fe} r_o}{h_{ie} + R_b}\right). \tag{5.115}$$

Algebraic manipulations on Equations (5.110) and (5.115) lead to:

$$A_I = \frac{h_{fe} r_o + h_{ie} + R_b}{\left(h_{fe} + 1\right) r_o + h_{ie} + R_b + R_c}. \tag{5.116}$$

The current gain remains essentially unchanged by the presence of non-zero h_{oe}. Small external resistances will very slightly increase the gain while extremely large R_c will decrease the gain slightly.

Voltage Gain

The output voltage can be determined through a voltage division between r_o and R_c in Figure 5.22:

$$v_o = \left(v_e - h_{fe} i_b r_o\right)\left(\frac{R_c}{R_c + r_o}\right). \tag{5.117}$$

The emitter voltage, v_e, and the base current, i_b, are related by h_{ie} and R_b through Equation (5.109). Substitution of this expression yields:

$$v_o = v_e\left(1 + \frac{h_{fe} r_o}{h_{ie} + R_b}\right)\left(\frac{R_c}{R_c + r_o}\right). \tag{5.118}$$

The voltage gain is easily obtained:

$$A_V = \frac{v_o}{v_e} = \left(1 + \frac{h_{fe} r_o}{h_{ie} + R_b}\right)\left(\frac{R_c}{R_c + r_o}\right) \approx \left(\frac{h_{fe} R_c}{h_{ie} + R_b}\right)\left(\frac{r_o}{R_c + r_o}\right). \tag{5.119}$$

The voltage gain is reduced by the presence of non-zero h_{oe}.

Output Resistance

The output resistance is the same as that seen for a common-emitter amplifier with an emitter resistor (Equation (5.75)). The external resistors have changed name so that the expression becomes:

$$R_o = \{R_s//(R_b + h_{ie})\} + r_o \left\{1 + \frac{h_{fe} R_s}{R_s + h_{ie} + R_b}\right\}. \tag{5.120}$$

This is a very large resistance.

5.6 COMPARISON OF BJT AMPLIFIER TYPES

Single-BJT amplifiers have been shown to fall into three general categories: Common-Emitter (both with and without an emitter resistor), Common-Collector, and Common-Base. The performance characteristics for each type of amplifier are summarized in Table 5.6.

Table 5.6: Qualitative comparison of BJT amplifier configurations

	CE	CE + R_e	CC	CB
A_I	High	High	High	≈ Unity
R_i	Medium	High	High	Low
A_V	High	Medium	≈ Unity	Medium to High
R_o	High	Very High	Low	Very High

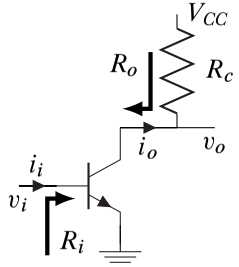
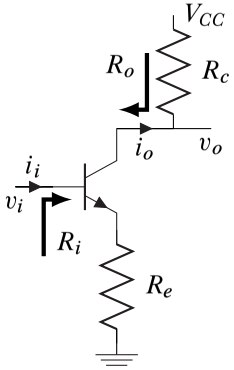
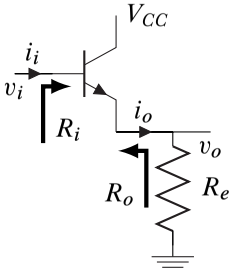
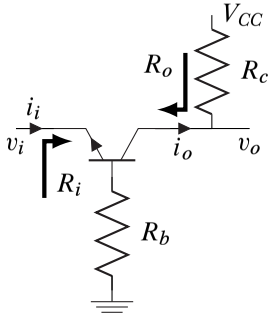
The common-emitter configuration appears the most useful of the three types: it provides both significant current and voltage gain (in each case with an inversion).

The common-emitter amplifier input and output impedances are high. In fact, this configuration is the most versatile of the three types and will often form the major gain portion of multiple-transistor amplifiers.

The common-collector and common-base configurations amplify either current or voltage, but not both. Neither inverts either the voltage or current signal. These configurations find greatest utility as impedance-matching (or buffer) stages of multi-stage amplifiers. Common-collector amplifier stages are capable of easily driving low-impedance loads. Common-base stages can impedance-match a very low-impedance source.

Quantitative expressions for the amplifier performance characteristics are found in Table 5.7. These expressions are based on the often realistic assumption concerning the relative size of the external resistors (connected to the collector and emitter terminals) and the BJT output resistance: $h_{oe}(R_e + R_c) \ll 1$. High resistance loads require the more exact expressions for amplifier performance that do not depend on that assumption. These expressions can be found in previous subsections concerning the effects of non-zero h_{oe}.

Table 5.7: Summary of bipolar junction transistor amplifier performance characteristics

	CE	CE + R_e	CC	CB
				
$A_I = \frac{i_o}{i_i}$	$-h_{fe}$	$-h_{fe}$	$h_{fe}+1$	$\frac{h_{fe}}{h_{fe}+1}$
$R_I = \frac{v_i}{i_i}$	h_{ie}	$h_{ie}+(h_{fe}+1)R_e$	$h_{ie}+(h_{fe}+1)R_e$	$\frac{h_{ie}+R_b}{h_{fe}+1}$
$A_V = \frac{v_o}{v_i}$	$\frac{-h_{fe}R_c}{h_{ie}}$	$\frac{-h_{fe}R_c}{h_{ie}+(h_{fe}+1)R_e}$	$1-\frac{h_{ie}}{R_i}$	$\frac{h_{fe}R_c}{h_{ie}+R_b}$
$R_o = \frac{v_o}{i_o}$	$\frac{1}{h_{oe}} \approx \infty$	$\approx \infty$	$\frac{R_b+h_{ie}}{h_{fe}+1}$	$\approx \infty$

5.7 FET LOW-FREQUENCY MODELS

The FET saturation region with small-signal input variations about the DC quiescent operating point (Q-point) is considered approximately linear in nature. Therefore, like the BJT, small-signal approximations, in the form of approximate circuit networks, are commonly used to model FET operation in the saturation region. The model is used to approximate all FET types.

Figure 5.23a shows a "generic" FET biased in the saturation region by a gate-source voltage V_{GSQ}, with a drain-source voltage V_{DSQ} and drain current I_{DQ}. The effect of small changes of the bias voltages on I_D can be found by independently varying V_{GSQ} and V_{DSQ} as shown in Figure 5.23b and c, respectively.

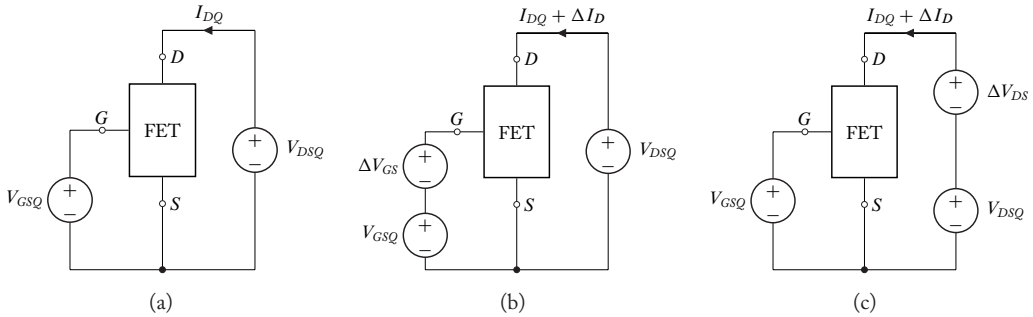


Figure 5.23: (a) Generic FET biased in the saturation region by a gate-source voltage V_{GSQ}, with a drain-source voltage V_{DSQ} and drain current I_{DQ}. (b) Method for determining gate small-signal transconductance with small variations in V_{GS} causing small changes in I_D. (c) Method for determining drain small-signal conductance with small variations in V_{DS} causing small changes in I_D.

The change in I_D with respect to small variations in V_{GS} and V_{DS} are expressed as conductance parameters. These parameters are:

1. *Small-signal transconductance or mutual conductance,* g_m, often referred to simply as "transconductance." The mathematical relation for determining transconductance corresponding to the measurement in Figure 5.23b is,

$$g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{constant}} \approx \left.\frac{\Delta I_D}{\Delta V_{GS}}\right|_{V_{DS}=\text{constant}}. \tag{5.121}$$

2. *Small-signal drain conductance* or *output conductance*, g_d. Corresponding to the measurement in Figure 5.23c, the output conductance is defined as,

$$g_d = r_d^{-1} = \left.\frac{\partial I_D}{\partial V_{DS}}\right|_{V_{GS}=\text{constant}} \approx \left.\frac{\Delta I_D}{\Delta V_{DS}}\right|_{V_{GS}=\text{constant}}, \tag{5.122}$$

where r_d^{-1} is the drain resistance or output resistance in Ohms.

Both g_m and g_d have units of conductance and are expressed in Siemens [S].

Consider the general case where both V_{DS} and V_{GS} changed simultaneously. The corresponding total change in the drain current is,

$$\Delta I_D = \left(\frac{\partial I_D}{\partial V_{GS}}\bigg|_{V_{DS}=\text{constant}} \right) \Delta V_{GS} + \left(\frac{\partial I_D}{\partial V_{DS}}\bigg|_{V_{GS}=\text{constant}} \right) \Delta V_{DS}. \tag{5.123}$$

If ΔI_D, ΔV_{DS}, and ΔV_{GS} are time-varying quantities about the Q-point they are AC signals. Equation (5.123) can then be re-written as:

$$i_d = \left(\frac{\partial i_D}{\partial v_{GS}}\bigg|_Q \right) v_{gs} + \left(\frac{\partial i_D}{\partial v_{DS}}\bigg|_Q \right) v_{ds}. \tag{5.124}$$

Substituting the small-signal conductances into Equation (5.124) yields,

$$i_d = g_m v_{gs} + g_d v_{ds}. \tag{5.125}$$

Recall from Chapter 4 (Book 1) that the gate current is assumed to be zero. Therefore,

$$\Delta I_G = 0. \tag{5.126}$$

Equations (5.125) and (5.126) relate small-signal quantities that can are represented by the small-signal equivalent circuit of Figure 5.24.

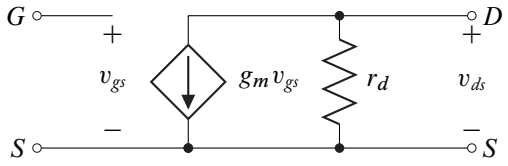


Figure 5.24: Low frequency small-signal model of an FET.

The voltage-controlled current source in the low frequency small-signal FET model in Figure 5.24 may be changed to a voltage-controlled voltage source by source transformation. The source transformed FET model is shown in Figure 5.25. The gain or amplification factor μ is defined as,

$$\mu = \frac{g_m}{g_d} = g_m r_d. \tag{5.127}$$

The FET models shown in Figures 5.24 and 5.25 are valid for all types of FETs biased in the saturation region. The actual values of the elements in the model vary for different FETs.

The value of $r_d = g_d^{-1}$ can be obtained from the output characteristic curve of the FET at the desired Q-point. From Equation (5.122), g_d is the slope of the line defined by I_D and V_{DS} at

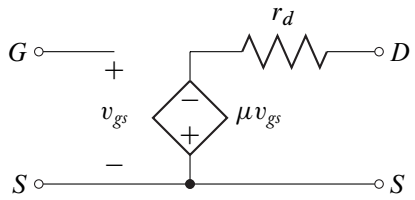


Figure 5.25: Equivalent low frequency model of a FET with a voltage-controlled voltage source.

the desired Q-point defined by a constant V_{GSQ},

$$g_d = \left.\frac{\Delta i_D}{\Delta v_{DS}}\right|_{V_{GSQ}} = r_d^{-1}. \tag{5.128}$$

Typical values for $r_d = g_d^{-1}$ range from 10 kΩ to 100 kΩ. r_d can also be determined from I_D and the Early voltage, V_A, using the following relationship:

$$r_d = \frac{V_A}{I_D}. \tag{5.128a}$$

The small-signal value for g_m for the JFET and depletion MOSFET is found by taking the derivative of I_D from Table 4.2 (Book 1) with respect to V_{GS},

$$\begin{aligned} g_m = \frac{\partial I_D}{\partial V_{GS}} &= \frac{\partial\left[I_{DSS}\left(1-\dfrac{V_{GS}}{V_{PO}}\right)^2\right]}{\partial V_{GS}} \\ &= \frac{-2I_{DSS}\left(1-\dfrac{V_{GS}}{V_{PO}}\right)}{V_{PO}} = 2\left(\frac{I_{DSS}}{V_{PO}^2}\right)(V_{GS}-V_{PO}). \end{aligned} \tag{5.129}$$

But, by definition,

$$I_D = I_{DSS}\left(1-\frac{V_{GS}}{V_{PO}}\right)^2 \quad \text{or} \quad I_{DSS} = \frac{I_D}{\left(1-\dfrac{V_{GS}}{V_{PO}}\right)^2}. \tag{5.130}$$

Substituting Equation (5.130) into (5.129) and simplifying yields an alternate expression for the small-signal transconductance of depletion type FETs:

$$g_m = \frac{2I_D}{(V_{GS}-V_{PO})} = 2\sqrt{I_D\left(\frac{I_{DSS}}{V_{PO}^2}\right)}. \tag{5.131a}$$

For the enhancement MOSFET, g_m is found by taking the derivative of I_D from Table 4.2 (Book 1) with respect to V_{GS},

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\partial [K(V_{GS} - V_T)^2]}{\partial V_{GS}}$$
$$= \frac{2I_D}{(V_{GS} - V_T)} = 2K\,(V_{GS} - V_T) = 2\sqrt{I_D K}. \tag{5.132}$$

Typical values for g_m range from 10^{-4} to 10^{-2} S.

An alternate method for arriving at the small-signal FET model is through the use of two-port analysis. The y-parameter two-port parameters are used since the independent variables are port voltages (V_{GS} and V_{DS}) and the dependent variable is the drain current I_D. As in the BJT, one terminal of the FET is assigned as a common terminal to both ports. In practice, the FET source is assigned as the common terminal.

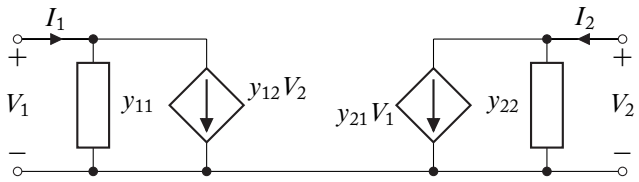


Figure 5.26: Generic y-parameter two port network.

The generic y-parameter two port network is shown in Figure 5.26. Recall the y-parameter equations from Equation (5.4) and (5.6):

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} y_{11} & y_{12} \\ y_{21} & y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix},$$

and

$$y_{ij} = \left.\frac{\partial I_i}{\partial V_j}\right|_{V_{k\neq j}=\text{constant}}.$$

For the FET, v_{gs} and v_{ds} are represented as V_1 and V_2 in the two-port network, respectively. The currents I_1 and I_2 are I_G and I_D, respectively. However, the gate current in the FET is approximately zero. Therefore, $I_1 = 0$, which implies that the dependent current source $y_{12}V_2 = 0$, and the two port network exhibits an infinite input impedance ($y_{11} = 0$). The remaining two parameters of the y-parameter two-port network the transadmittance y_{21} and the output admittance y_{22}. The real components of the transadmittance and output admittance were found in Equations (5.121) and (5.122):

$$|y_{21}| = g_m \tag{5.133}$$

and

$$|y_{22}| = g_d \tag{5.134}$$

y-parameters with descriptive subscripts are often used to specify parameters in manufacturers' data sheets. The second subscript defines which terminal is chosen as common (the source), and the first subscript identifies the function of the parameter:

$$y_{fs} = |y_{21}| = g_m = \text{ input admittance—source as common terminal (5.133)}$$
$$y_{os} = |y_{22}| = g_d = \text{ output admittance—source as common terminal (5.134).}$$

The small-signal parameters for the FET are summarized in Table 5.8. The FET parameters are dependent on quiescent conditions.

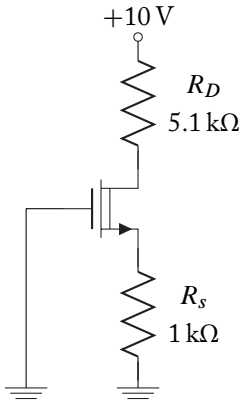
Table 5.8: FET small-signal parameters

Small-Signal Parameter	Value
JFET and Depletion MOSFET: g_m	$2\left(\frac{I_{DSS}}{V_{PO}^2}\right)(V_{GS} - V_{PO}) = \frac{2I_D}{V_{GS} - V_{PO}} = 2\sqrt{I_D\left(\frac{I_{DSS}}{V_{PO}^2}\right)}$
Enhancement MOSFET: g_m	$2K(V_{GS} - V_T) = \frac{2I_D}{V_{GS} - V_T} = 2\sqrt{I_D K}$
All FETs: r_d	$\left\|\frac{V_A}{I_D}\right\|$

Example 5.10
Given a depletion NMOSFET with parameters:

$$I_{DSS} = 5\,\text{mA} \qquad V_{PO} = -2\,\text{V},$$

operating in the circuit shown, determine the small-signal transconductance for the FET.



Solution:

The quiescent conditions must first be obtained. Note that $V_G = 0$. Therefore,

$$V_{GS} = V_G - V_S = -V_S = -I_D(1000).$$

Solving for V_{DS},

$$\begin{aligned} V_{DS} &= 10 - I_D(1000 + 5100) \\ &= 10 - I_D(6100). \end{aligned}$$

Assume that the FET is in saturation. That is,

$$V_{DS} > V_{GS} - V_{PO}.$$

Then,

$$\begin{aligned} I_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_{PO}}\right)^2 \\ &= I_{DSS}\left(1 + \frac{I_D \times 10^3}{V_{PO}}\right)^2 \\ &= 5 \times 10^{-3}\,(1 - 500 I_D)^2 = 5 \times 10^{-3}\left(1 - 1000 I_D + 250 \times 10^3 I_D^2\right). \end{aligned}$$

Use the quadratic equation to solve for I_D. The two roots of the second order equation are:

$$I_D = 1.07\,\text{mA or } 3.725\,\text{mA}.$$

For $I_D = 1.07\,\text{mA}$,

$$V_{GS} = -I_D(1\,\text{K}) = -1.07 \times 10^{-3}(1000) = -1.07\,\text{V},$$

and

$$\begin{aligned} V_{DS} &= 10 - I_D(6.1\,\text{k}) \\ &= 10 - 1.07 \times 10^{-3}(6100) \\ &= 3.47\,\text{V}. \end{aligned}$$

Similarly, for $I_D = 3.725\,\text{mA}$,

$$V_{GS} = -I_D(1\,\text{k}) = -3.725 \times 10^{-3}(1000) = -3.725\,\text{V},$$

and

$$\begin{aligned} V_{DS} &= 10 - I_D(6100) \\ &= 10 - 3.725 \times 10^{-3}(6100) \\ &= -12.7\,\text{V}. \Leftarrow \text{This solution is clearly not valid.} \end{aligned}$$

Therefore, the drain current is $I_D = 1.07\,\text{mA}$.

Confirm that the FET is in saturation:

$$V_{DS} > V_{GS} - V_{PO} = -1.07 + 2 = 0.93\,\text{V},$$

and

$$3.47\,\text{V} > 0.93\,\text{V}. \Leftarrow \text{The FET is in saturation.}$$

The transconductance of the FET is

$$g_m = \frac{-2I_D}{(V_{PO} - V_{GS})} = \frac{-2\left(1.07 \times 10^{-3}\right)}{-2 - (-1.07)} = 2.3\,\text{mS}.$$

5.8 COMMON-SOURCE AMPLIFIERS

Between the ohmic and cut-off regions of the FET characteristics lies a linear region where the variation in the output voltage about the quiescent point is directly proportional to the variation in the input voltage. This section develops the characteristics of the common-source amplifier using the small-signal parameters developed in Section 5.7.

Common-source amplifiers have the following general circuit topology:

- the input signal enters the FET at the gate,
- the output signal exits the FET at the drain, and
- the source terminal is connected to a constant voltage, often the ground (common) terminal, sometimes with an intervening resistor.

A simple common-source amplifier is shown in Figure 5.27. Although a enhancement NMOSFET amplifier is shown, the small-signal analysis of the amplifier is valid for all types of FETs. As in BJT amplifiers, the quiescent point of the FET must be set with circuitry external to the transistor so that it is in the FET saturation region. The values of the resistors, R_D and R_G, and the DC voltage sources, V_{GG} and V_{DD}, have therefore been chosen so that the FET is in the saturation region and the circuit will operate as an amplifier. Since the gate current is zero, $V_{GG} = V_G$ and the gate to source voltage, V_{GS}, must have a value that places the operation of the FET in the saturation region. The voltage source, v_S, is a small-signal AC source with source resistance R_S.

One the quiescent conditions ($v_s = 0$) have been calculated, and it has been determined that the FET is in the saturation region, the significant small-signal conductances can be calculated by referring to Table 5.8.

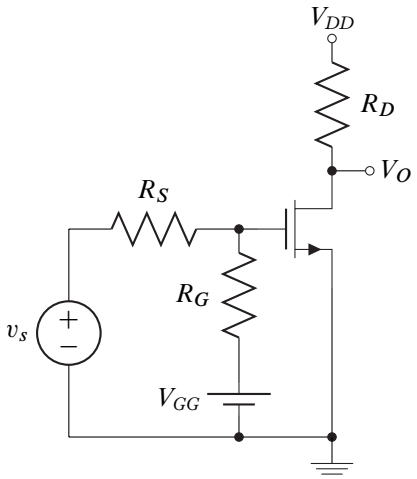


Figure 5.27: A simple common-source amplifier.

For the enhancement NMOSFET,

$$\begin{aligned} g_m &= 2K\,(V_{GS} - V_T) = 2\sqrt{I_D K} \\ \text{and} \qquad g_d &= \left.\frac{\Delta i_D}{\Delta v_{DS}}\right|_{V_{GSQ}} \qquad \text{from the characteristic curves.} \end{aligned} \tag{5.135}$$

The small-signal circuit performance can now be calculated. Total circuit performance is the sum of the quiescent and small-signal performance. The process of AC modeling of the circuit and replacing the FET with an appropriate AC model, applied to Figure 5.27, is shown in Figure 5.28.

The small-signal performance can be obtained from analysis of the circuit of Figure 5.28b. The small-signal characteristics that are of interest are: *the input resistance*, *the voltage gain*, and *the output resistance*. Definitions of these quantities may vary due to differing definition of the exact location of the point of measurement.

Input Resistance

The input resistance (shown in Figure 5.28b) is given by:

$$R_i \equiv \frac{v_{gs}}{i_g} = \infty. \tag{5.136}$$

Because the gate current is zero, the input impedance is infinite.

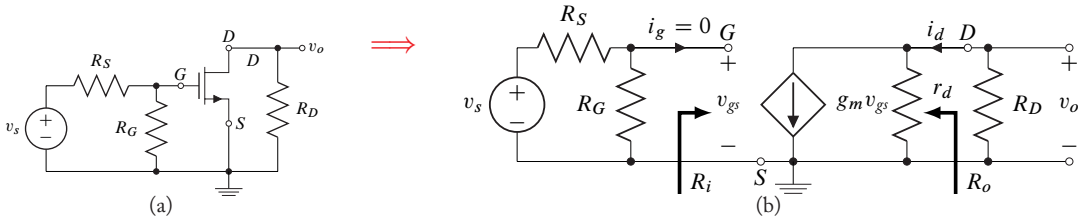


Figure 5.28: AC modeling of a common-source amplifier. (a) The small-signal circuit: DC sources set to zero. (b) FET replaced by the small-signal model.

Voltage Gain

The voltage gain is the ratio of output voltage to input voltage. If the input voltage is taken to be the voltage input to the FET, v_g,

$$A_V \equiv \frac{v_o}{v_g}. \tag{5.137}$$

Using previously introduced methods to calculate the voltage gain yields,

$$A_V = \frac{v_o}{v_g} = \frac{v_o}{v_{gs}} = \left(\frac{v_o}{i_l}\right)\left(\frac{i_l}{v_{gs}}\right), \tag{5.138}$$

where $i_l \equiv$ the current through the parallel combination of the load resistor R_D and r_d. But

$$i_l = -g_m v_{gs}. \tag{5.139}$$

Therefore, the voltage gain is,

$$A_V = (R_D//r_d)\left(\frac{-g_m v_{gs}}{v_{gs}}\right) = -g_m\,(R_D//r_d)\,. \tag{5.140}$$

The voltage gain from the source is of interest as well. This overall voltage gain can be defined as:

$$A_{VS} \equiv \frac{v_o}{v_s}. \tag{5.141}$$

This ratio can be directly derived from the voltage gain, A_V, and a voltage division between the source resistance, R_S, and the bias resistance, R_G (the amplifier input resistance, R_i, is infinite),

$$A_{VS} = \frac{v_o}{v_s} = \left(\frac{v_o}{v_{gs}}\right)\left(\frac{v_{gs}}{v_s}\right) = A_V\left(\frac{(R_G//R_i)}{(R_G//R_i)+R_S}\right) = A_V\left(\frac{R_G}{R_G+R_S}\right). \tag{5.142}$$

The appropriate substitutions lead to,

$$A_{VS} = -g_m\,(r_d//R_D)\left(\frac{R_G}{R_G+R_S}\right). \tag{5.143}$$

Output Resistance

The output resistance is defined as the Thévenin resistance at the output of the amplifier looking back into the amplifier. The circuit of Figure 5.29 defines the necessary topology and circuit variables for output resistance calculations.

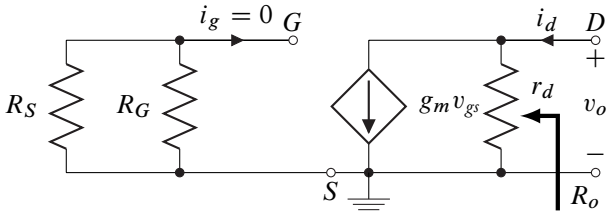


Figure 5.29: Circuit for calculating the output resistance of the common-source amplifier.

Since $i_g = 0$, the dependent source is also zero-valued and the output resistance is the parallel combination of r_d and the resistance of the zero-valued dependent source,

$$R_O = r_d // \infty = r_d \left| \frac{V_A}{I_D} \right|, \tag{5.144}$$

where V_A is the Early voltage of the FET and I_D is the quiescent drain current.

The output resistance is dependent on the quiescent conditions of the FET. It is also possible to define the output resistance of a common-source amplifier to include the drain resistor, R_D,

$$R_{Ol} = R_O // R_D = r_d // R_D. \tag{5.145}$$

Example 5.11

Given an n-JFET with parameters:

$$V_{PO} = -5\,\text{V} \qquad V_A = 100\,\text{V}$$
$$I_{DSS} = 6\,\text{mA} \qquad I_S = 1\,\text{pA}$$

operating in the circuit shown at room temperature, determine the amplifier small signal performance characteristics in its midband frequency range.

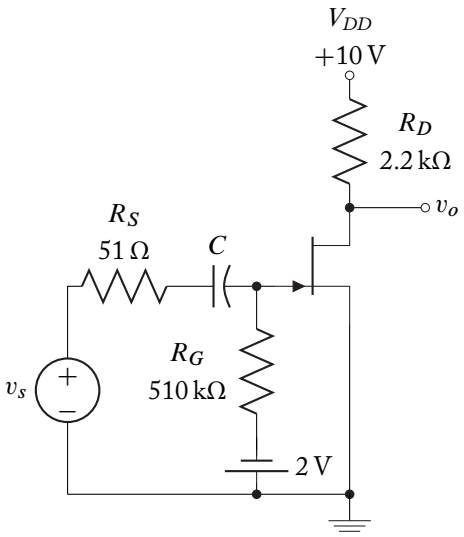
Solution:

The modeling process for FET circuit performance contains the following steps:

1. Determine the quiescent (DC) conditions - verify FET in saturation region.
2. Determine the FET AC model parameters from the quiescent conditions.
3. Create the AC equivalent circuit.

4. Determine the AC performance by replacing the FET by its AC model.

5. Add the results of the DC and AC analysis to obtain total circuit performance.



Step #1 Determine the circuit quiescent (DC) conditions - verify that the FET is in the saturation region. Using the equations in Table 4.2 (Book 1) for the n-JFET,

$$V_{GS} = V_G - V_S = -2 - 0 = -2V$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{PO}}\right)^2 = 6 \times 10^{-3}\left(1 - \frac{-2}{-5}\right)^2 = 2.16 \text{ mA}.$$

So the drain-source voltage is

$$V_{DS} = V_{DD} - I_D R_D = 10 - \left(2.16 \times 10^{-3}\right)(2200) = 5.25 \text{ V}.$$

The condition for saturation is

$$V_{DS} \geq V_{GS} - V_{PO} = -2 - (-5) = 3 \text{ V}$$
$$5.25 \text{ V} > 3 \text{ V}.$$

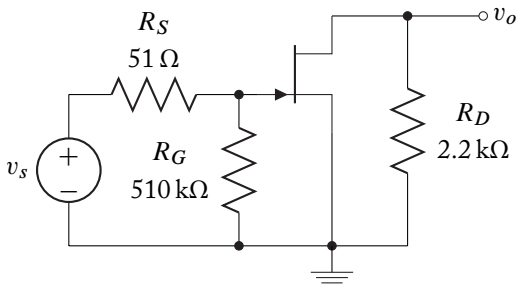
The circuit is confirmed to be in saturation.

Step #2 Determine the FET AC model parameters from the quiescent conditions. The relevant parameters are:

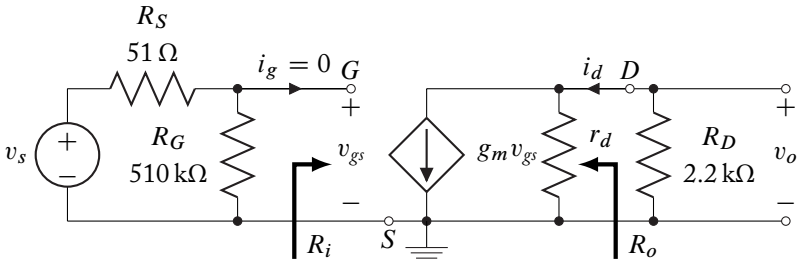
$$r_d = \frac{V_A}{I_D} = \frac{100}{2.16 \times 10^{-3}} = 46.3\ \text{k}\Omega$$

$$g_m = \frac{-2I_{DSS}\left(1 - \dfrac{V_{GS}}{V_{PO}}\right)}{V_{PO}} = \frac{-2\left(6 \times 10^{-3}\right)\left(1 - \dfrac{-2}{-5}\right)}{-5} = 1.44\ \text{mS}.$$

Step #3 Create an AC equivalent circuit. The DC sources are set to zero and the output voltage becomes a small-signal quantity.



Step #4 Determine the AC performance by replacing the FET by its AC model. The small-signal circuit model of the amplifier is shown below.



The input resistance to the gate of the FET is,

$$R_i = \infty.$$

If the input resistance is measured to the left of R_S then,

$$R_{iS} = R_S + (R_G // R_i) = 51 + 510\,\text{k} \approx 510\,\text{k}\Omega.$$

The voltage gain from the gate of the FET is,

$$A_V = -g_m\,(r_d // R_D) = -1.44 \times 10^{-3}\,(46.3\,\text{k}//2200) = -3.$$

The voltage gain from the source is given by,

$$A_{VS} = -g_m\,(r_d//R_D)\left(\frac{R_G}{R_G+R_S}\right)$$
$$= -1.44\times10^{-3}\,(46.3\,\text{k}//2.2\,\text{k})\left(\frac{510\,\text{k}}{510\,\text{k}+51}\right)\approx A_V=-3.$$

The output resistance is,

$$R_O = r_d//\infty = r_d = \left|\frac{V_A}{I_D}\right| = \left|\frac{100}{2.16\times10^{-3}}\right| = 46.3\,\text{k}\Omega.$$

If the drain resistance is included in the output resistance,

$$R_{Ol} = R_O//R_D = r_d//R_D = 46.3\,\text{k}//2.2\,\text{k} = 2.1\,\text{k}\Omega.$$

Step #6 is beyond the requirements of this problem, but all the data is present to add the quiescent solution to the small-signal solution for total circuit response.

5.8.1 COMMON-SOURCE AMPLIFIERS WITH NON-ZERO SOURCE RESISTANCE

Several characteristics of the common-source amplifier (Figure 5.30) can be altered through the addition of a resistor connected between the source and common (ground). The source resistor has the following effects on common-source amplifiers:

- increased output resistance
- decreased voltage gain

Derivation of these effects follows the process described in Section 5.7.

In order to determine the AC performance of this amplifier, the quiescent conditions must first be obtained. If the FET is operating in the saturation region, an AC equivalent model of the circuit can be obtained (Figure 5.31a) and the FET can be replaced by its small-signal model (based on the quiescent conditions) in the AC equivalent circuit (Figure 5.31b). Circuit performance can then be obtained from this equivalent circuit.

Input Resistance

The input resistance (shown in Figure 5.31b) is the same as the input resistance for a common-source amplifier without a source resistor,

$$R_i = \infty. \tag{5.146}$$

The addition of a source resistor has not changed the input resistance of the amplifier.

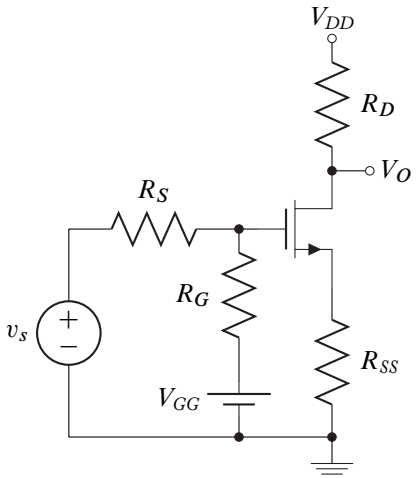


Figure 5.30: A common-source amplifier with source resistor.

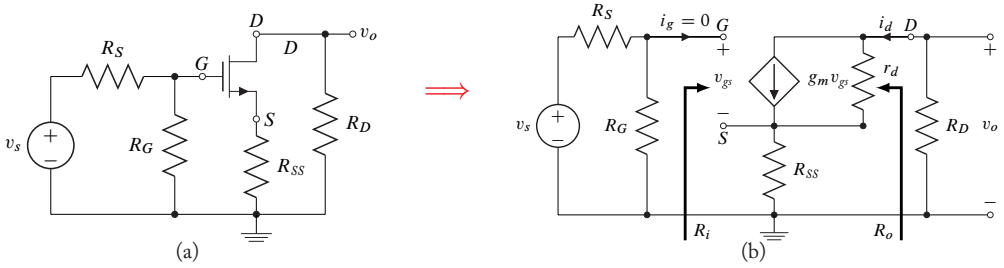


Figure 5.31: AC modeling of a common-source amplifier with a source resistor. (a) The small-signal circuit : DC sources set to zero. (b) The FET replaced by the small-signal model.

Voltage Gain

The voltage gain is the ratio of the output voltage to input voltage. If the input voltage is again taken to be the voltage at the input to the FET, v_g,

$$A_V \equiv \frac{v_o}{v_g}. \tag{5.146}$$

Although the voltage gain can be found using the small-signal model of Figure 5.31b, the alternate source-transformed form of the FET small-signal model of Figure 5.25 may be used. The small-signal model of the common-source amplifier with source resistor using the small-signal model of the FET with voltage-controlled voltage source is shown in Figure 5.32.

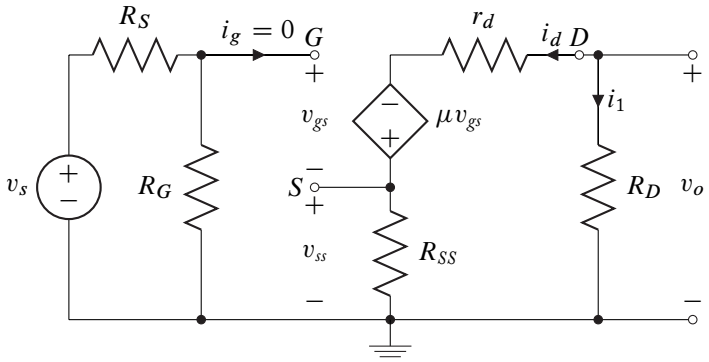


Figure 5.32: Alternate small-signal model of the common-source amplifier with source resistor using the small-signal model of the FET with voltage-controlled voltage source.

Using the methods similar to those of the simple common-source amplifier to calculate the voltage gain yields,

$$A_V = \left(\frac{v_o}{v_g}\right) = \left(\frac{v_o}{i_l}\right)\left(\frac{i_l}{v_{gs}}\right)\left(\frac{v_{gs}}{v_g}\right). \tag{5.147}$$

Knowing that $\mu = g_m r_d$, Equation (5.147) is,

$$\begin{aligned} A_v &= (R_D)\left(\frac{-\dfrac{g_m v_{gs} r_d}{R_{SS} + r_d + R_D}}{v_{gs}}\right)\left(\frac{v_{gs}}{v_g}\right) \\ &= -\frac{g_m r_d R_D}{R_{SS} + r_d + R_D}\left(\frac{v_{gs}}{v_g}\right). \end{aligned} \tag{5.148}$$

By voltage division, the source voltage, v_{ss}, is

$$v_{ss} = \frac{g_m v_{gs} r_d R_{SS}}{R_{SS} + r_d + R_D}. \tag{5.149}$$

Using Equation (5.149), the gate-source voltage is,

$$v_{gs} = v_g - v_{ss} = v_g - \frac{g_m v_{gs} r_d R_{SS}}{R_{SS} + r_d + R_D}. \tag{5.150}$$

From Equation (5.150), the expression for the gate voltage, v_g, as a function of the gate-source voltage, v_{gs}, is,

$$v_g = v_{gs}\left(1 + \frac{g_m r_d R_{SS}}{R_{SS} + r_d + R_D}\right). \tag{5.151}$$

Substituting Equation (5.151) into (5.148) results in the expression for the voltage gain for the common-source amplifier with FET source terminal resistor,

$$\begin{aligned} A_V &= -\frac{g_m r_d R_D}{R_{SS} + r_d + R_D} \left(\frac{v_{gs}}{v_{gs}\left(1 + \dfrac{g_m v_{gs} r_d R_{SS}}{R_{SS} + r_d + R_D}\right)} \right) \\ &= -\frac{g_m r_d R_D}{R_{SS} + r_d + R_D} \left(\frac{1}{\left(\dfrac{r_d + R_D + (1 + g_m r_d) R_{SS}}{R_{SS} + r_d + R_D}\right)} \right) \\ &= -\frac{g_m r_d R_D}{r_d + R_D + (1 + g_m r_d) R_{SS}}. \end{aligned} \tag{5.152}$$

The voltage gain from the input voltage source is defined as:

$$A_{VS} \equiv \frac{v_o}{v_s}. \tag{5.153}$$

This ratio can be directly derived from the voltage gain following the derivation for the common-source amplifier *without* source resistor:

$$A_{VS} = \frac{v_o}{v_s} = \left(\frac{v_o}{v_g}\right)\left(\frac{v_g}{v_s}\right) = A_V \left(\frac{v_g}{v_s}\right). \tag{5.154}$$

Using voltage division to determine v_g as a function of v_s,

$$\begin{aligned} A_{VS} = A_V \left(\frac{v_g}{v_s}\right) &= A_V \left(\frac{\dfrac{v_s R_G}{R_G + R_S}}{v_s} \right) \\ &= -\frac{g_m r_d R_D}{r_d + R_D + (1 + g_m r_d) R_{SS}} \left(\frac{R_G}{R_G + R_S}\right). \end{aligned} \tag{5.155}$$

Output Resistance

The output resistance is defined as the Thévenin resistance at the output of the amplifier looking back into the amplifier. As in the case of the simple common-source amplifier, R_o is measured without considering R_D.

Calculations to determine the output resistance of the common-source amplifier with source resistor are based on the small-signal model of Figure 5.31b and is similar to the calculations performed previously for the common-source amplifier without source resistor. The circuit of Figure 5.33 defines the necessary topology and circuit variables for output resistance calculations.

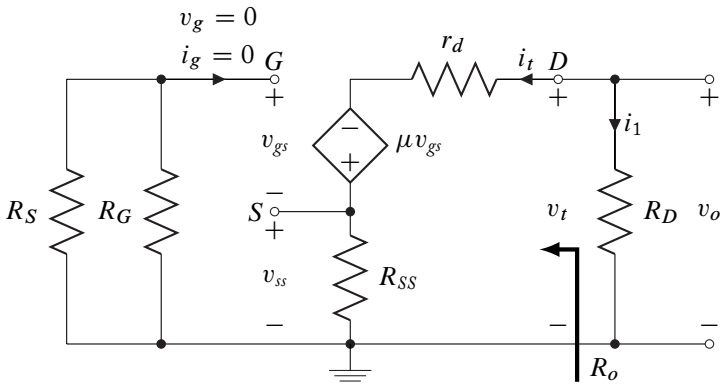


Figure 5.33: Circuit for calculating the output resistance of the common-source amplifier with source resistor.

The Thévenin voltage and current at the output are v_t and i_t, respectively, where the output resistance, R_o, is the Thévenin resistance defined as,

$$R_o = \frac{v_t}{i_t}. \tag{5.156}$$

Solving for the Thévenin current as a function of the Thévenin voltage,

$$i_t = \frac{v_t + g_m v_{gs} r_d}{r_d + R_{SS}} = \frac{v_t + g_m r_d \left(v_g - v_{ss}\right)}{r_d + R_{SS}}. \tag{5.157}$$

Since R_S and the gate bias resistor, R_G, are grounded (the independent voltage source is set to zero), $v_g = 0$. Therefore, Equation (5.157) is,

$$i_t = \frac{v_t - g_m r_d v_{ss}}{r_d + R_{SS}}. \tag{5.158}$$

The voltage at the source of the FET, v_{ss}, is simply,

$$v_{SS} = i_t R_{SS}. \tag{5.159}$$

Substituting Equation (5.159) into (5.158) yields,

$$i_t = \frac{v_t - g_m r_d \left(i_t R_{SS}\right)}{r_d + R_{SS}}. \tag{5.160}$$

Rearranging Equation (5.160) and solving for the Thévenin voltage, v_t, in terms of the Thévenin current, i_t,

$$v_t = i_t \left[r_d + \left(1 + g_m r_d\right) R_{SS}\right]. \tag{5.161}$$

Applying the definition of the Thévenin resistance shown in Equation (5.156) to (5.161) yields the output resistance,

$$R_o = \frac{v_t}{i_t} = [r_d + (1 + g_m r_d) R_{SS}]. \tag{5.162}$$

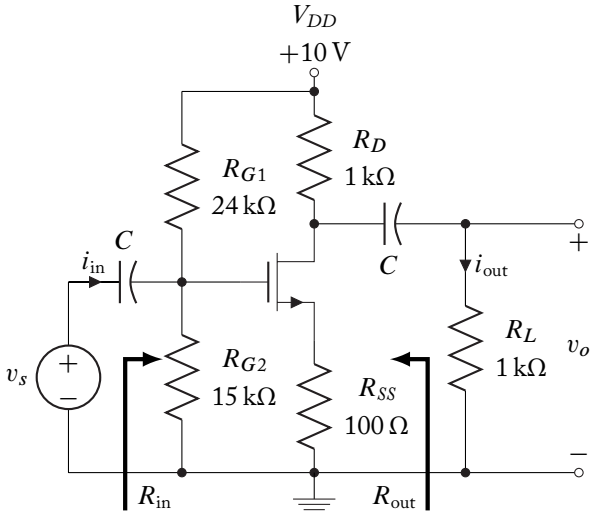
Example 5.12

An enhancement NMOSFET with parameters:

$$K = 2.96 \times 10^{-3}\,\text{A/V}^2$$
$$V_T = 2\,\text{V} \qquad r_d = 30\,\text{k}\Omega$$

is placed in the amplifier shown. Assume that the amplifier is operating in its midband frequency range with quiescent point

$$I_D = 5\,\text{mA}.$$



Determine the following circuit parameters:

$$A_{VS} = \frac{v_o}{v_s},\ R_{in},\ \text{and}\ R_{out}.$$

Solution:

The quiescent point of the FET must be found first to ensure that it is in the saturation region. For DC operation, all capacitors appear as open circuits. By voltage division, the gate voltage is

$$V_G = \frac{V_{DD} R_{G2}}{R_{G1} + R_{G2}} = \frac{10\,(15\,\text{k})}{24\,\text{k} + 15\,\text{k}} \approx 3.8\,\text{V}.$$

The voltage at the source terminal of the FET is,

$$V_S = I_D R_{SS} = \left(5 \times 10^{-3}\right)(100) = 0.5\,\text{V}.$$

Therefore, the gate-source voltage is,

$$V_{GS} = V_G - V_S = 3.8 - 0.5 = 3.3\,\text{V}.$$

The drain source voltage is,

$$V_{DS} = V_{DD} - I_D\,(R_D + R_{SS}) = 10 - 5 \times 10^{-3}\,(1100) = 4.5\,\text{V}.$$

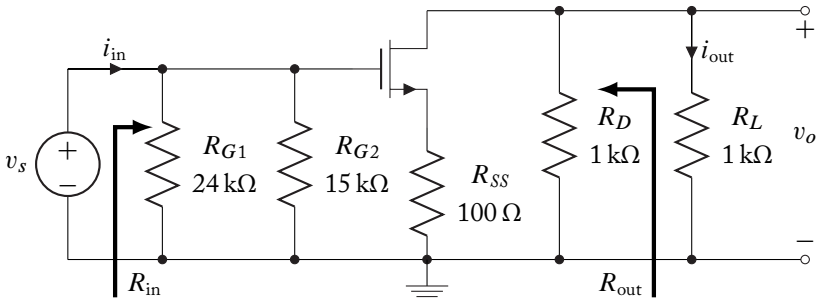
For the FET to be in saturation, $V_{DS} \geq V_{GS} - V_T$. For the circuit in this example,

$$\begin{aligned} 4.5\,\text{V} &> 3.3\,\text{V} - 2\,\text{V} \\ &> 1.3\,\text{V} \quad \Rightarrow \quad \text{the FET is in saturation.} \end{aligned}$$

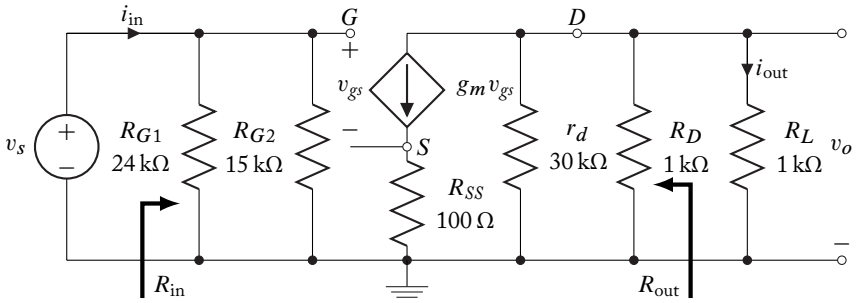
The small-signal transconductance is,

$$g_m = 2\sqrt{I_D K} = 2\sqrt{\left(5 \times 10^{-3}\right)\left(2.96 \times 10^{-3}\right)} \approx 7.7\,\text{mS}.$$

The AC equivalent circuit can be found by setting all DC sources to zero and, since the circuit is in its midband frequency range, all capacitors are replaced by short circuits.



The AC equivalent circuit leads to the small-signal equivalent circuit for the amplifier:



$$
\begin{aligned}
A_{VS} = A_V &= -\frac{g_m r_d R_D}{R_{SS} + r_d + R_D + g_m r_d R_{SS}} \\
&= -\frac{7.7 \times 10^{-3}\,(30\,\text{k})\,(1\,\text{k})}{100 + 30\,\text{k} + 1\,\text{k} + 7.7 \times 10^{-3}\,(30\,\text{k})\,(100)} \approx -4.3 \\
R_{in} &= 24\,\text{k}//15\,\text{k} = 9.23\,\text{k}\Omega \\
R_{out} &= R_D // R_o = R_D // (r_d + R_{SS} + g_m r_d R_{SS}) \\
&= 1\,\text{k}//\left[30\,\text{k} + 100 + 7.7 \times 10^{-3}\,(30\,\text{k})\,(100)\right] \approx 980\,\Omega.
\end{aligned}
$$

Summary of Common-source Amplifier Properties

A summary of common-source amplifier performance characteristics, as derived in this section, is given in Table 5.9.

Table 5.9: Common-source amplifier characteristics

Parameter	CS	CS $+R_{SS}$
R_i	∞	∞
A_V	$-g_m(R_D // r_d)$	$-\dfrac{g_m r_d R_D}{r_d + R_D + (1 + g_m r_d)R_{SS}}$
R_o	r_d	$r_d + (1 + g_m r_d)R_{SS}$

5.9 COMMON-DRAIN AMPLIFIERS

Common-drain amplifiers have the following general circuit topology:

- the input signal enters the FET at the gate,
- the output signal exits the FET at the source, and
- the drain terminal is connected to a constant voltage, often the ground (common) terminal, sometimes with an intervening resistor.

A simple common-drain amplifier is shown in Figure 5.34. Although Figure 5.34 shows a common-drain n-JFET amplifier, the small-signal analysis of the amplifier is valid for all types of FETs. As in BJT amplifiers, the quiescent point of the FET must be set with circuitry external to the transistor insuring linear operation which for the FET is the saturation region. The values of the resistors, R_D and R_G, and the DC voltage sources, V_{GG} and V_{DD}, have therefore been chosen so that the FET is in the saturation region and the circuit will operate as an amplifier. Since the gate current is zero, $V_{GG} = V_G$ and the gate to source voltage, V_{GS}, must have a value that places the operation of the FET in the saturation region. The voltage source, v_S, is a small-signal AC source with source resistance R_S.

Once the quiescent conditions ($v_s = 0$) have been calculated, and it has been determined that the FET is in the saturation region, the significant small-signal conductances can be calculated by referring to Table 5.8.

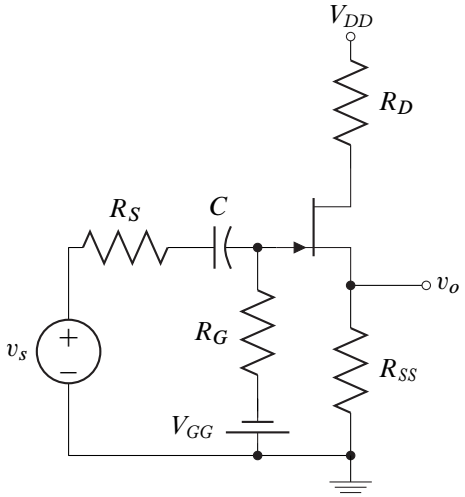


Figure 5.34: A simple common-drain amplifier.

For the n-JFET,

$$g_m = \frac{2I_D}{(V_{GS} - V_{PO})}$$

and (5.163)

$$g_d = \frac{\Delta i_D}{\Delta v_{DS}}\bigg|_{V_{GSQ}} = \frac{|I_{DQ}|}{|V_A|}$$

from the characteristic curves, where V_A is the Early voltage.

The small-signal circuit performance can now be calculated. Total circuit performance is the sum of the quiescent and small-signal performance. The process of AC modeling of the circuit and replacing the FET with an appropriate AC model, applied to Figure 5.34, is shown in Figure 5.35.

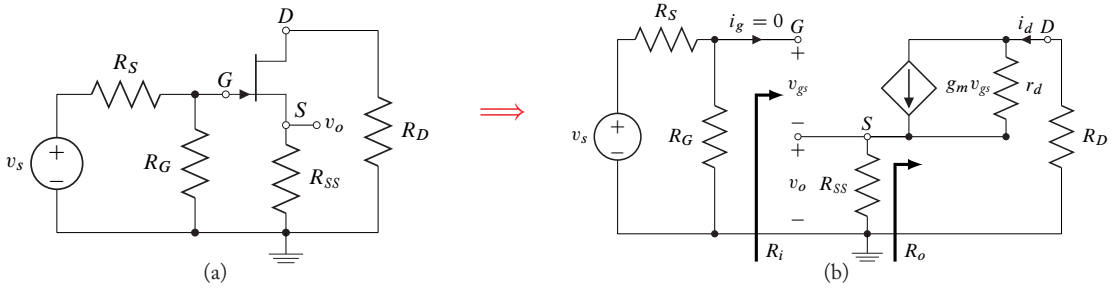


Figure 5.35: AC modeling of a common-drain amplifier. (a) The small-signal circuit: DC sources set to zero. (b) FET replaced by the small-signal model.

The small-signal performance can be obtained from analysis of the circuit of Figure 5.35b. The small-signal characteristics that are of interest are: *the input resistance*, *the voltage gain*, and *the output resistance*. Definitions of these quantities may vary due to differing definition of the exact location of the point of measurement.

Input Resistance

The input resistance (shown in Figure 5.35b) is given by:

$$R_i \equiv \frac{v_{gs}}{i_g} = \infty. \tag{5.164}$$

Because the gate current is zero, the input impedance is infinite.

Voltage Gain

The voltage gain is the ratio of the output voltage to input voltage. If the input voltage is again taken to be the voltage at the input to the FET, v_g,

$$A_V \equiv \frac{v_o}{v_g}. \tag{5.165}$$

Although the voltage gain can be found using the small-signal model of Figure 5.35b, the alternate source-transformed form of the FET small-signal model of Figure 5.36 may be used. The small-signal model of the common source amplifier with source resistor using the small-signal model of the FET with voltage-controlled voltage source is shown in Figure 5.36.

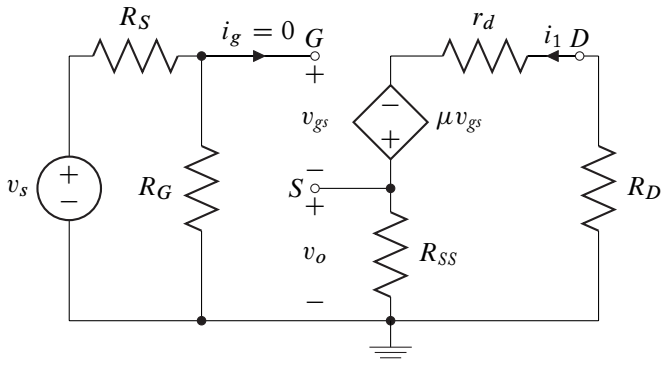


Figure 5.36: Alternate small-signal model of the common-drain amplifier using the small-signal model of the FET with voltage-controlled voltage source.

Using the methods similar to those of the simple common source amplifier with source resistor to calculate the voltage gain yields,

$$A_V = \left(\frac{v_o}{v_g}\right) = \left(\frac{v_o}{i_l}\right)\left(\frac{i_l}{v_{gs}}\right)\left(\frac{v_{gs}}{v_g}\right). \tag{5.166}$$

Knowing that $\mu = g_m r_d$, Equation (5.166) is,

$$\begin{aligned} A_v &= (R_{SS})\left(\frac{\dfrac{g_m v_{gs} r_d}{R_{SS} + r_d + R_D}}{v_{gs}}\right)\left(\frac{v_{gs}}{v_g}\right) \\ &= \frac{g_m r_d R_{SS}}{R_{SS} + r_d + R_D}\left(\frac{v_{gs}}{v_g}\right). \end{aligned} \tag{5.167}$$

By voltage division, the output voltage, v_o, is

$$v_o = \frac{g_m v_{gs} r_d R_{SS}}{R_{SS} + r_d + R_D}. \tag{5.168}$$

Using Equation (5.168), the gate-source voltage is,

$$v_{gs} = v_g - v_o = v_g - \frac{g_m v_{gs} r_d R_{SS}}{R_{SS} + r_d + R_D}. \tag{5.169}$$

From Equation (5.169), the expression for the gate voltage, v_g, as a function of the gate-source voltage, v_{gs}, is,

$$v_g = v_{gs}\left(1 + \frac{g_m r_d R_{SS}}{R_{SS} + r_d + R_D}\right). \tag{5.170}$$

Substituting Equation (5.170) into (5.167) results in the expression for the voltage gain for the common-drain amplifier,

$$\begin{aligned} A_V &= \frac{g_m r_d R_{SS}}{R_{SS} + r_d + R_D}\left(\frac{v_{gs}}{v_{gs}\left(1 + \dfrac{g_m v_{gs} r_d R_{SS}}{R_{SS} + r_d + R_D}\right)}\right) \\ &= \frac{g_m r_d R_{SS}}{R_{SS} + r_d + R_D}\left(\frac{1}{\left(\dfrac{r_d + R_D + R_{SS}(1 + g_m r_d)}{R_{SS} + r_d + R_D}\right)}\right) \\ &= \frac{g_m r_d R_{SS}}{r_d + R_D + R_{SS}(1 + g_m r_d)}. \end{aligned} \tag{5.171}$$

For $g_m r_d R_{SS} \gg R_D + r_d$ then $A_V \approx 1$. The common-drain configuration is therefore called the source follower, since the output follows the input voltage. The common-drain amplifier is the FET counterpart to the BJT common collector amplifier.

The voltage gain from the input voltage source is defined as:

$$A_{VS} \equiv \frac{v_o}{v_s}. \tag{5.172}$$

This ratio can be directly derived from the voltage gain following the derivation for the common-source amplifier:

$$A_{VS} = \frac{v_o}{v_s} = \left(\frac{v_o}{v_g}\right)\left(\frac{v_g}{v_s}\right) = A_V\left(\frac{v_g}{v_s}\right). \tag{5.173}$$

Using voltage division to determine v_g as a function of v_s,

$$\begin{aligned} A_{VS} &= A_V\left(\frac{v_g}{v_s}\right) = A_V\left(\frac{\dfrac{v_s R_G}{R_G + R_S}}{v_s}\right) \\ &= \frac{g_m r_d R_{SS}}{r_d + R_D + R_{SS}(1 + g_m r_d)}\left(\frac{R_G}{R_G + R_S}\right) \\ &\approx \frac{R_G}{R_G + R_S}, \qquad g_m r_d R_{SS} \gg R_D + r_d. \end{aligned} \tag{5.174}$$

Output Resistance

The output resistance is defined as the Thévenin resistance at the output of the amplifier looking back into the amplifier. Calculations to determine the output resistance of the common-drain amplifier are based on the small-signal model of Figure 5.36 and are similar to the calculations performed previously for the common source amplifier with source resistor. The circuit of Figure 5.37 defines the necessary topology and circuit variables for output resistance calculations.

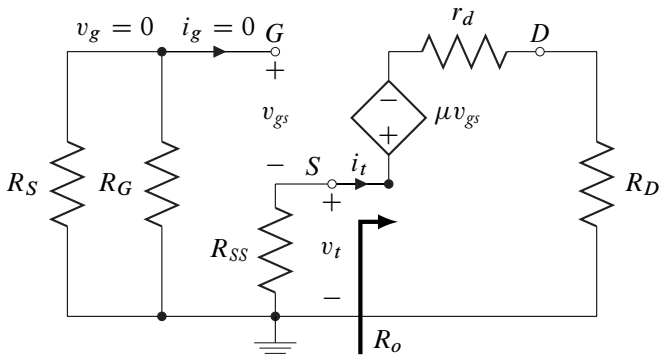


Figure 5.37: Circuit for calculating the output resistance of the common-drain amplifier.

The Thévenin voltage and current at the output are v_t and i_t, respectively, where the output resistance, R_o, is the Thévenin resistance defined as,

$$R_o = \frac{v_t}{i_t}. \tag{5.175}$$

Solving for the Thévenin current as a function of the Thévenin voltage,

$$i_t = \frac{v_t - g_m v_{gs} r_d}{r_d + R_D} = \frac{v_t - g_m r_d\left(v_g - v_t\right)}{r_d + R_D}. \tag{5.176}$$

Since R_S and the gate bias resistor, R_G, are grounded (the independent voltage source is set to zero), $v_g = 0$. Therefore, Equation (5.176) is,

$$i_t = \frac{v_t + g_m r_d v_t}{r_d + R_D}. \tag{5.177}$$

Rearranging Equation (5.177) and solving for the Thévenin voltage, v_t, in terms of the Thévenin current, i_t,

$$i_t = \frac{v_t\,(1 + g_m r_d)}{r_d + R_D}. \tag{5.178}$$

Applying the definition of the Thévenin resistance shown in Equation (5.175) to (5.178) yields the output resistance,

$$R_o = \frac{v_t}{i_t} = \frac{r_d + R_D}{1 + g_m r_d}. \tag{5.179}$$

The output resistance of the common-drain amplifier is typically small.

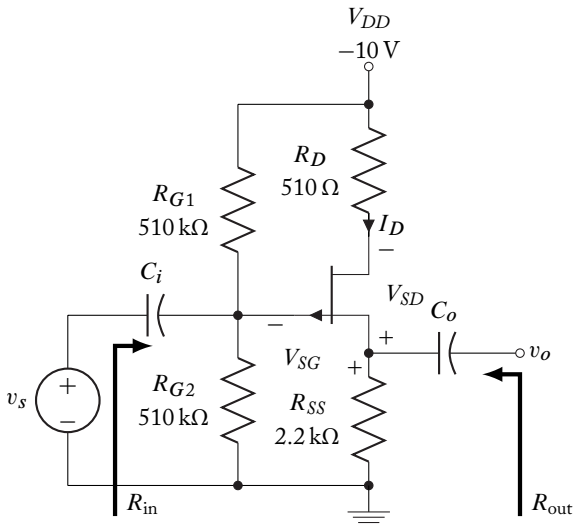
Example 5.13

Given a p-JFET with parameters:

$$V_{PO} = 3\,\text{V} \qquad r_d = 30\,\text{k}\Omega$$
$$I_{DSS} = -13.8\,\text{mA}$$

operating at room temperature in the circuit shown, is placed in the amplifier shown. Assume that the amplifier is operating in its midband frequency range, and determine the following circuit parameters:

$$A_{VS} = \frac{v_o}{v_s},\ R_{in},\ \text{and}\ R_{out}.$$



Solution:

The quiescent point of the FET must be found first to ensure that it is in the saturation region. For DC operation, all capacitors appear as open circuits. By voltage division, the gate voltage is

$$V_G = \frac{V_{DD} R_{G2}}{R_{G1} + R_{G2}} = \frac{-10\,(510\,\text{k})}{510\,\text{k} + 510\,\text{k}} \approx -5\,\text{V}.$$

The drain current, I_D, is

$$\begin{aligned} I_D &= I_{DSS}\left(1 - \frac{V_{GS}}{V_{PO}}\right)^2 = I_{DSS}\left(1 - \frac{-V_{SG}}{V_{PO}}\right)^2 \\ &= -13.8 \times 10^{-3}\left(1 - \frac{-(V_{SG})}{3}\right)^2, \end{aligned}$$

but

$$V_{SG} = V_S - V_G = I_D R_{SS} - V_G.$$

Substituting into the equation for I_D in terms of I_{DSS},

$$\begin{aligned} I_D &= -13.8 \times 10^{-3}\left(1 - \frac{-(I_D R_{SS} - V_G)}{3}\right)^2 \\ &= -13.8 \times 10^{-3}\left(1 - \frac{-(2200 I_D + 5)}{3}\right)^2. \end{aligned}$$

By rearranging the equation, the drain current can be found by solving the second order polynomial equation:

$$0 = I_D^2 + 7.41 \times 10^{-3} I_D + 13.2 \times 10^{-6}.$$

Using the quadratic equation, the solutions to the drain current are:

$$I_D \approx \begin{cases} -3.0\ \text{mA} \\ -4.4\ \text{mA} \end{cases}.$$

To determine which of the two solutions for I_D are valid, test the values in the KVL equation for the source-drain loop,

$$0 = I_D\,(R_{SS} + R_D) - V_{SD} - V_{DD},$$

or

$$V_{SD} = I_D\,(R_{SS} + R_D) - V_{DD}$$

where $V_{DD} = -10\,\text{V}$.

For $I_D = -4.4\,\text{mA}$, the resultant $V_{SD} = -1.92\,\text{V}$. Since $V_{SD} < 0$, this result clearly indicates that the FET is not in saturation. Additionally, since V_{SG} is,

$$V_{SG} = V_S - V_G = I_D R_{SS} - V_G = \left(-4.4 \times 10^{-3}\right)(2200) - (-5) = -4.68\,\text{V}$$

and $V_{SG} < -V_{PO}$, the FET is in cut-off.

For $I_D = -3.0\,\text{mA}$, the resultant $V_{SD} = 1.87\,\text{V}$. Additionally, since

$$V_{SG} = V_S - V_G = I_D R_{SS} - V_G = \left(-3.0 \times 10^{-3}\right)(2200) - (-5) = -1.6\,\text{V}$$

and

$$V_{SD} \geq V_{SG} + V_{PO}$$

or

$$1.87 \geq -1.6 + 3 = 1.4\,\text{V}$$

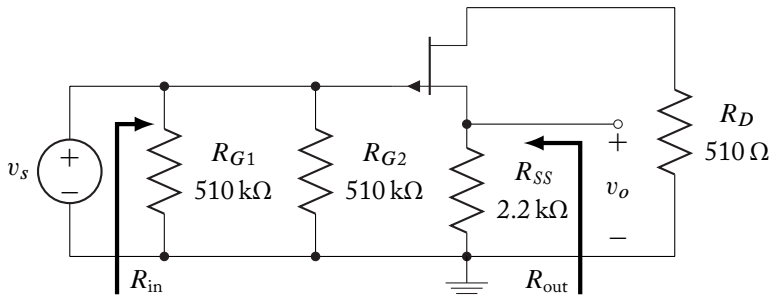
the FET is in saturation. Therefore, the valid solution for the drain current is,

$$I_D = -3.0\,\text{mA}.$$

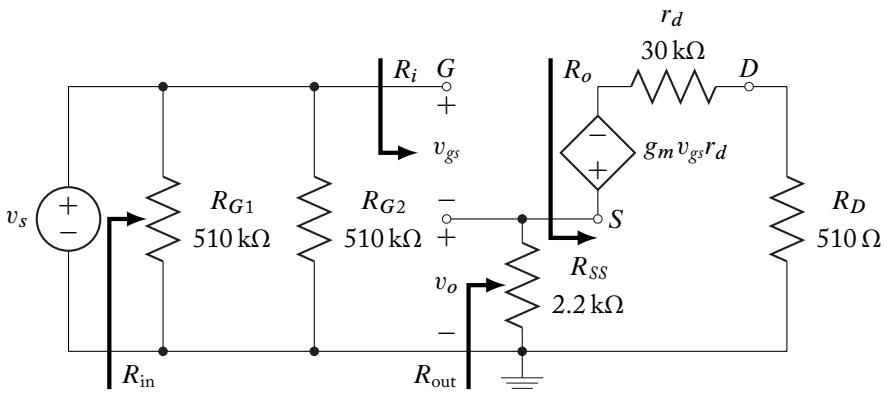
The small-signal transconductance is,

$$g_m = \frac{2I_D}{(V_{GS} - V_{PO})} = \frac{2\left(-3 \times 10^{-3}\right)}{[-(-1.6) - 3]} \approx 4.3\ \text{mS}.$$

The AC equivalent circuit can be found by setting all DC sources to zero and, since the circuit is in its midband frequency range, all capacitors are replaced by short circuits.



The small-signal models for p- and n-channel devices are identical and are based on the Q-points determined by the external circuitry. The AC equivalent circuit leads to the small-signal equivalent circuit for the p-channel JFET common-drain amplifier:



The voltage gain of the amplifier is,

$$A_{VS} = A_V\left(\frac{v_g}{v_s}\right) = A_V\left(\frac{\dfrac{v_s R_G}{R_G + R_S}}{v_s}\right)$$
$$= \frac{g_m r_d R_{SS}}{r_d + R_D + R_{SS}(1 + g_m r_d)}\left(\frac{R_G}{R_G + R_S}\right).$$

But since $R_S = 0$, the gain of the amplifier is,

$$A_{VS} = A_V = \frac{g_m r_d R_{SS}}{R_{SS} + r_d + R_D + g_m r_d R_{SS}}$$
$$= \frac{\left(4.3 \times 10^{-3}\right)(30\,\text{k})(2.2\,\text{k})}{30\,\text{k} + 510 + (2.2\,\text{k})\left[1 + \left(4.3 \times 10^{-3}\right)(30\,\text{k})\right]} = 0.896 \approx 0.90.$$

Here R_{in} is given as

$$R_{in} = R_i // (R_{G1} // R_{G2}) = \infty // (510\,\text{k} // 510\,\text{k}) = 255\,\text{k}\Omega$$

and R_{out} as,

$$R_{out} = R_o // R_{SS} = \left(\frac{r_d + R_D}{1 + g_m r_d}\right) // R_{SS}$$
$$= \left[\frac{30\,\text{k} + 510}{1 + \left(4.3 \times 10^{-3}\right)(30\,\text{k})}\right] // 2.2\,\text{k} = 235 // 2.2\,\text{k} = 212\,\Omega.$$

A summary of common-drain amplifier performance characteristics, as derived in this section, is given in Table 5.10.

Table 5.10: Common-drain amplifier characteristics

	CD
R_i	∞
A_V	$\dfrac{g_m r_d R_{SS}}{r_d + R_D + R_{SS}(1 + g_m r_d)}$ $\approx 1, \quad g_m r_d R_{SS} \gg R_D r_d$
R_o	$\dfrac{r_d + R_D}{1 + g_m r_d}$

5.10 COMMON-GATE AMPLIFIERS

Common-gate amplifiers have the following general circuit topology:

- the input signal enters the FET at the source,
- the output signal exits the FET at the drain, and
- the gate terminal is connected to a constant voltage, often the ground (common) terminal, sometimes with an intervening resistor.

A simple common-gate amplifier is shown in Figure 5.38. Although Figure 5.38 shows a common-gate depletion NMOSFET amplifier, the small-signal analysis of the amplifier is valid for all types of FETs. As in BJT amplifiers, the quiescent point of the FET must be set with circuitry external to the transistor so that it is in the FET saturation region. The values of the resistors, R_D and R_G, and the DC voltage sources, V_{GG} and V_{DD}, have therefore been chosen so that the FET is in the saturation region and the circuit will operate as an amplifier. Since the gate current is zero, $V_{GG} = V_G$ and the gate to source voltage, V_{GS}, must have a value that places the operation of the FET in the saturation region. The voltage source, v_S, is a small-signal AC source with source resistance R_S. Once the quiescent conditions ($v_s = 0$) have been calculated, and it has been determined that the FET is in the saturation region, the significant small-signal conductances can be calculated by referring to Table 5.8.

For the depletion NMOSFET,

$$g_m = \frac{2I_D}{(V_{GS} - V_{PO})}$$
$$\text{and} \qquad g_d = \left.\frac{\Delta i_D}{\Delta v_{DS}}\right|_{V_{GSQ}} = \frac{|I_{DQ}|}{|V_A|} \tag{5.180}$$

from the characteristic curves, where V_A is the Early voltage.

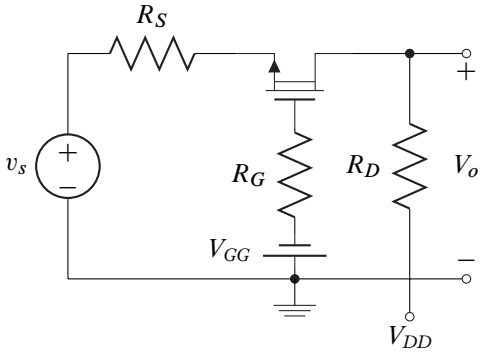


Figure 5.38: A simple common-gate amplifier.

The small-signal circuit performance can now be calculated. Total circuit performance is the sum of the quiescent and small-signal performance. The process of AC modeling of the circuit and replacing the FET with an appropriate AC model, applied to Figure 5.38, is shown in Figure 5.39.

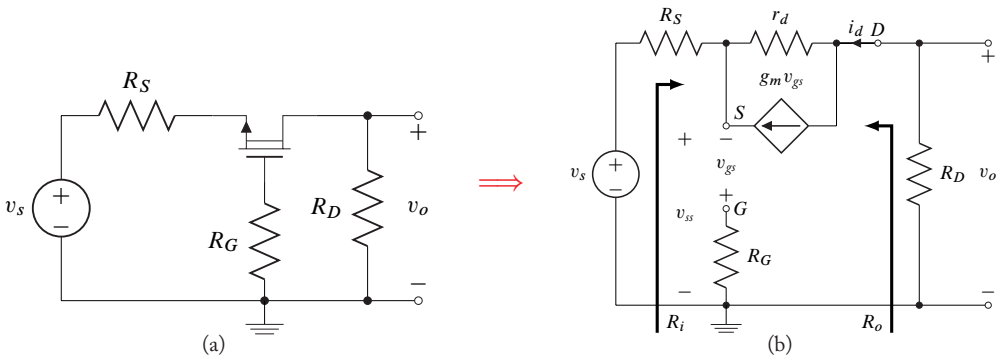


Figure 5.39: AC modeling of a common-gate amplifier. (a) The small-signal circuit: DC sources set to zero. (b) FET replaced by the small-signal model.

To simplify the analysis of the circuit, the source-transformed version of the FET model of Figure 5.40 is used to obtain the small-signal performance of the amplifier. The small-signal characteristics that are of interest are: *the input resistance*, *the voltage gain*, and *the output resistance*. Definitions of these quantities may vary due to differing definition of the exact location of the point of measurement.

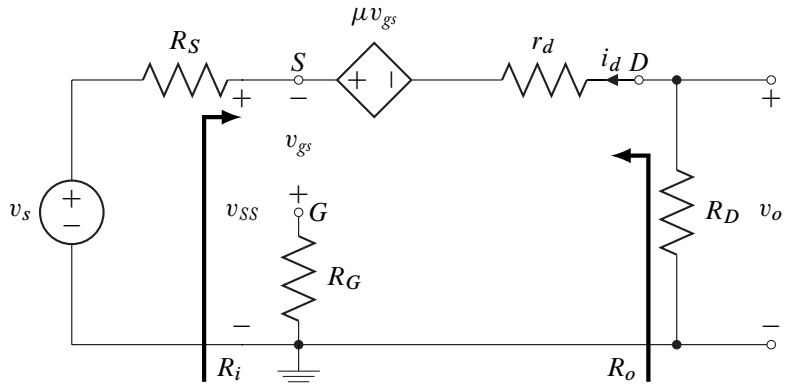


Figure 5.40: Alternate small-signal model of the common-gate amplifier using the small-signal model of the FET with voltage-controlled voltage source.

Input Resistance

The input resistance is defined as the Thévenin resistance at the input of the amplifier looking back into the amplifier. Calculations to determine the input resistance of the common-gate amplifier are based on the small-signal model of Figure 5.41 and are similar to the calculations performed previously for the common source amplifier with source resistor. The circuit of Figure 5.41 defines the necessary topology and circuit variables for output resistance calculations.

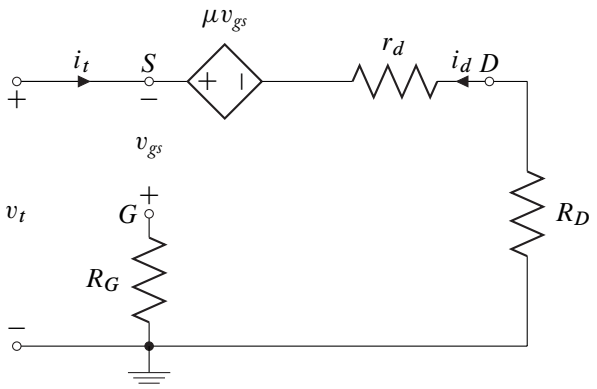


Figure 5.41: Circuit for calculating the input resistance of the common-gate amplifier.

The Thévenin voltage and current at the input are v_t and i_t, respectively, where the input resistance, R_i, is the Thévenin resistance defined as,

$$R_i = \frac{v_t}{i_t}. \tag{5.181}$$

Solving for the Thévenin current as a function of the Thévenin voltage,

$$i_t = \frac{v_t - g_m v_{gs} r_d}{r_d + R_D} = \frac{v_t - g_m r_d \left(v_g - v_t\right)}{r_d + R_D}. \tag{5.182}$$

Since the gate bias resistor, R_G, is grounded (the independent voltage source is set to zero), $v_g = 0$. Therefore, Equation (5.176) is,

$$i_t = \frac{v_t + g_m r_d v_t}{r_d + R_D}. \tag{5.183}$$

Rearranging Equation (5.183) and solving for the Thévenin voltage, v_t, in terms of the Thévenin current, i_t,

$$i_t = \frac{v_t \left(1 + g_m r_d\right)}{r_d + R_D}. \tag{5.184}$$

Applying the definition of the Thévenin resistance shown in Equation (5.181) to (5.184) yields the input resistance,

$$R_i = \frac{v_t}{i_t} = \frac{r_d + R_D}{1 + g_m r_d}. \tag{5.185}$$

The input resistance of the common-gate amplifier is typically small, and is identical to the output resistance of the common drain amplifier.

Voltage Gain

The voltage gain is the ratio of the output voltage to input voltage. If the input voltage is taken to be the voltage at the input to the FET, v_{ss},

$$A_V \equiv \frac{v_o}{v_{ss}}. \tag{5.186}$$

Although the voltage gain can be found using the small-signal model of Figure 5.39b, the alternate source-transformed form of the FET small-signal model of Figure 5.40 may be used.

Using the methods discussed for other FET amplifier configurations to calculate the voltage gain yields,

$$A_V = \left(\frac{v_o}{v_{ss}}\right) = \left(\frac{v_o}{-i_d}\right)\left(\frac{-i_d}{v_{ss}}\right). \tag{5.187}$$

Knowing that $\mu = g_m r_d$, Equation (5.187) is,

$$A_v = (R_D)\left(\frac{\dfrac{v_{ss} - g_m v_{gs} r_d}{r_d + R_D}}{v_{ss}}\right). \tag{5.188}$$

The gate-source voltage is,

$$v_{gs} = v_g - v_{ss} = 0 - v_s = -v_{ss}. \tag{5.189}$$

Substituting Equation (5.189) into (5.188) results in the expression for the voltage gain for the common-gate amplifier,

$$A_v = \frac{(1 + g_m r_d)\, R_D}{r_d + R_D}. \tag{5.190}$$

Output Resistance

The output resistance is defined as the Thévenin resistance at the output of the amplifier looking back into the amplifier. Calculations to determine the output resistance of the common-gate amplifier are based on the small-signal model of Figure 5.40. The circuit of Figure 5.42 defines the necessary topology and circuit variables for output resistance calculations.

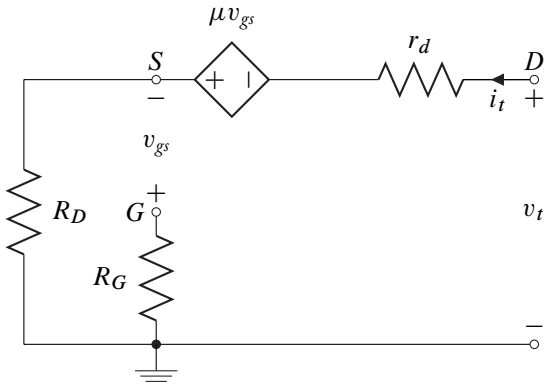


Figure 5.42: Circuit for calculating the output resistance of the common-gate amplifier.

The Thévenin voltage and current at the output are v_t and i_t, respectively, where the output resistance, R_o, is the Thévenin resistance defined as,

$$R_o = \frac{v_t}{i_t}. \tag{5.191}$$

Solving for the Thévenin current as a function of the Thévenin voltage,

$$i_t = \frac{v_t + g_m v_{gs} r_d}{r_d + R_S} = \frac{v_t + g_m r_d \left(v_g - i_t R_S\right)}{r_d + R_S}. \tag{5.192}$$

Since the gate bias resistor, R_G, is grounded (the independent voltage source is set to zero), $v_g = 0$. Therefore, Equation (5.192) is,

$$i_t = \frac{v_t - i_t g_m r_d R_S}{r_d + R_S}. \tag{5.193}$$

Rearranging Equation (5.193) and solving for the Thévenin voltage, v_t, in terms of the Thévenin current, i_t,

$$i_t = \frac{v_t}{r_d + R_S + g_m r_d R_S}. \tag{5.194}$$

Applying the definition of the Thévenin resistance shown in Equation (5.191) to (5.194) yields the output resistance,

$$R_o = R_S + r_d + g_m r_d R_S. \tag{5.195}$$

The output resistance of the common-gate amplifier is typically large.

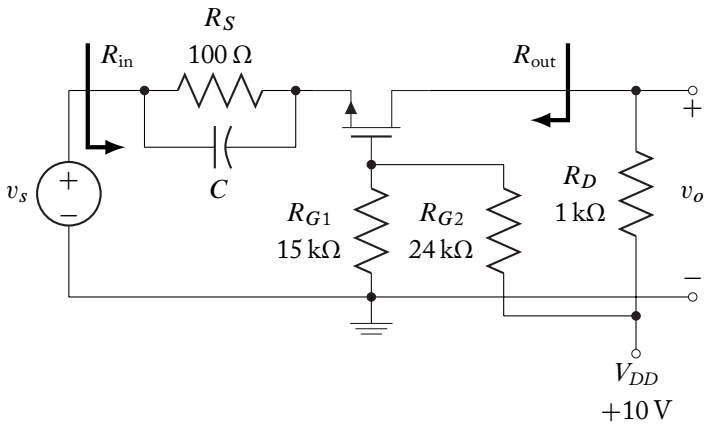
Example 5.14
An enhancement NMOSFET with parameters:

$$V_T = 2\,\text{V}, \qquad r_d = 30\,\text{k}\Omega$$
$$K = 2.96\,\text{mA/V}^2$$

is placed in the amplifier shown so that the quiescent operating point is $I_D = 5\,\text{mA}$.

Assume that the amplifier is operating in its midband frequency range, and determine the following parameters:

$$A_{VS} = \frac{v_O}{v_S},\ R_{in},\ \text{and}\ R_{out}.$$



Solution:

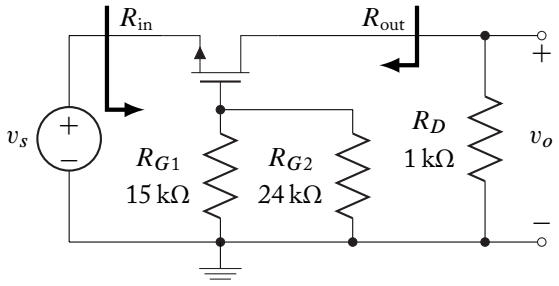
The quiescent point of the FET must be the same as was found in Example 5.12:

$$V_{GS} = 3.3\,\text{V} \qquad V_{DS} = 4.5\,\text{V}$$

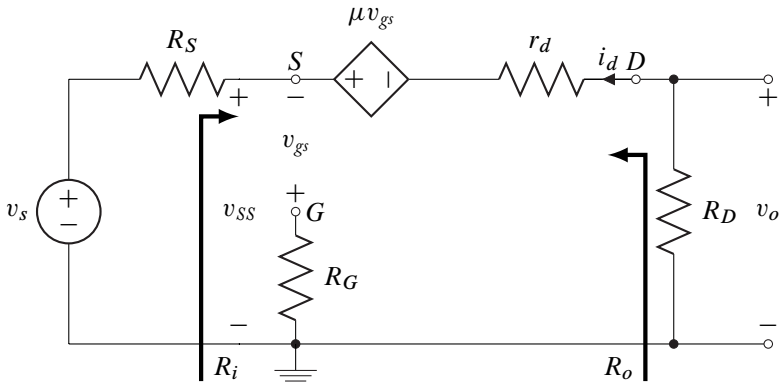
and the FET is in saturation. The small-signal transconductance is,

$$g_m = 2\sqrt{I_D K} = 2\sqrt{\left(5 \times 10^{-3}\right)\left(2.96 \times 10^{-3}\right)} \approx 7.7\,\text{mS}.$$

Since the circuit is in its midband frequency range, all capacitors are replaced by short circuits.



The AC equivalent circuit leads to the small-signal equivalent circuit for the common-gate amplifier:



The voltage gain of this amplifier is,

$$A_{VS} = A_V = \frac{(1 + g_m r_d)\, R_D}{r_d + R_D} = \frac{\left[\left(1 + \left(7.7 \times 10^{-3}\right)(30\,\text{k})\right)(1\,\text{k})\right]}{30\,\text{k} + 1\,\text{k}} \approx 7.5.$$

Here R_{in} is given as

$$R_{in} = R_i // R_D = \frac{r_d + R_D}{1 + g_m r_d} // R_D = \frac{30\,\text{k} + 1\,\text{k}}{1 + \left(7.7 \times 10^{-3}\right)(30\,\text{k})} // 1\,\text{k} \approx 134\,\Omega$$

and R_{out} as

$$\begin{aligned} R_{out} &= \left[r_d + R_S\,(1 + g_m r_d)\right] // R_D \\ &= \left[r_d + R_S\,(1 + g_m r_d)\right] // R_D. \end{aligned}$$

But $R_S = 0$, so

$$R_{out} = \frac{r_d + R_D}{1 + g_m r_d} = 968\,\Omega.$$

A summary of common-gate amplifier performance characteristics, as derived in this section, is given in Table 5.11.

Table 5.11: Common-gate amplifier characteristics

	CG
R_i	$\frac{r_d + R_D}{1 + g_m r_d}$
A_V	$\frac{(1 + g_m r_d) R_D}{r_d + R_D}$
R_o	$R_S + r_d + g_m r_d R_S$

5.11 COMPARISON OF FET AMPLIFIER TYPES

Single FET amplifiers have been shown to fall into three general categories: Common-Source (both with and without a source resistor), Common-Collector, and Common-Base. The performance characteristics for each type of amplifier are summarized in Table 5.12.

Table 5.12: Qualitative comparison of FET amplifier configurations

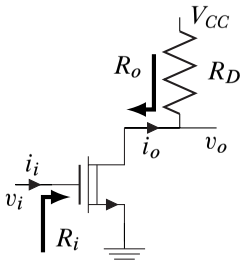
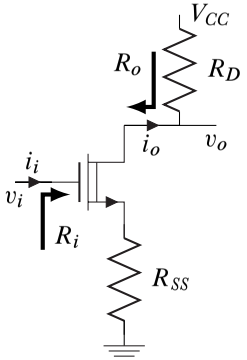
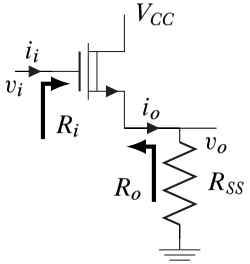
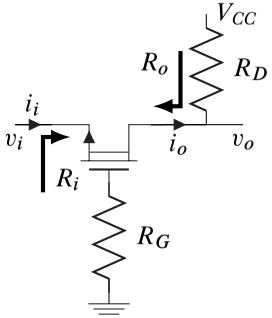
	CS	CS + R_S	CD	CG
R_i	Very High	Very High	Very High	Low
A_V	High	Medium	≈ Unity	Medium to High
R_o	High	Very High	Low	High

The common-source configuration appears the most useful of the three types: it provides significant voltage gain with inversion. The common-source amplifier input and output resistances are high. In fact, this configuration is the most versatile of the three types and will often form the major voltage gain stage portion of multiple-transistor amplifiers.

The common-drain configuration is, for all practical purposes, a unity gain, non-inverting buffer amplifier for impedance matching between electronic circuit stages. Common-drain amplifiers are capable of easily driving low resistance loads. Common-gate amplifiers can act as an impedance matching stage from low to high resistance electronic circuit stages.

Quantitative expressions for the amplifier performance are found in Table 5.13.

Table 5.13: Summary of field effect transistor amplifier performance characteristics

	CS	CS + R_{SS}	CD	CG
				
$R_I = \frac{v_i}{i_i}$	∞	∞	∞	$\frac{r_d + R_D}{1 + g_m r_d}$
$A_V = \frac{v_o}{v_i}$	$-g_m(R_D // r_d)$	$-\frac{g_m r_d R_D}{r_d + R_D + R_{SS}(1 + g_m r_d)}$	$\frac{g_m r_d R_{SS}}{r_d + R_D + R_{SS}(1 + g_m r_d)}$	$\frac{(1 + g_m r_d) R_D}{r_d + R_D}$
$R_o = \frac{v_o}{i_o}$	r_d	$r_d + R_{SS}(1 + g_m r_d)$	$\frac{r_d + R_D}{1 + g_m r_d}$	$r_d + R_{SS}(1 + g_m r_d)$

5.12 BIASING TO ACHIEVE MAXIMUM SYMMETRICAL SWING

Amplification can be restricted by the size and positioning of the available undistorted output swing. Amplifiers consisting strictly of a transistor and resistors can be biased so that the transistor quiescent point lies in the middle of the linear output voltage range provided by the power supply. This location of the Q-point allows symmetrical excursion of signal voltages about a central value: distortion (amplifier saturation) will occur for equal magnitude excursions in the positive and negative directions.

Amplifiers that have capacitively coupled loads or resistors that are shunted by capacitors in the output voltage/current relationship do not have the entire range of the power supply for output voltage swing. Placing the Q-point in the middle of the power supply rails will not provide equal output voltage swing and will greatly limit the utility of the amplifier. It is therefore important to be able to easily choose a Q-point that will provide the maximum symmetrical swing for the amplifier given the various design constraints.

A technique that analytically determines the Q-point for maximum symmetrical swing is based on transistor output load lines. The output curve for a transistor (either BJT or FET) is typically given as a current vs. voltage curve. On this curve DC and AC load lines can be drawn as shown in Figure 5.43.

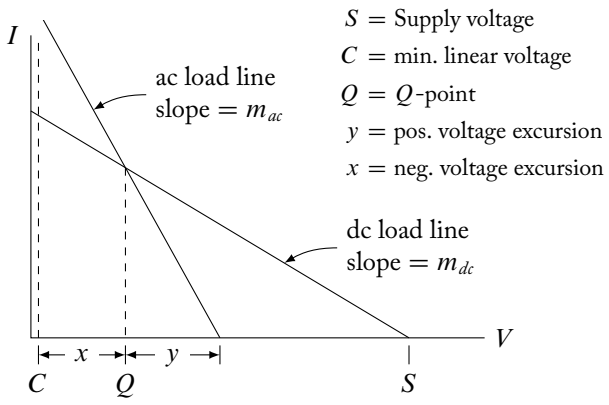


Figure 5.43: Typical amplifier AC and DC load lines.

The two load lines always intersect at the quiescent point: if there is zero AC, the output must be on the Q-point of the DC load line. It is also true that the magnitude of the midband AC load line for all practical amplifier circuits is greater than that of the DC load line. The increased magnitude AC load line slope decreases the available oscillatory swing along the abscissa to a value often significantly less than the power supply limits. The maximum supply limit {S} is typically

the magnitude of the power supply: the minimum supply limit {C} is determined by the edge of the linear region of the transistor (for a BJT it is approximately $V_{CE(sat)}$).

For maximum symmetrical swing it is necessary to choose a Q-point that allows equal oscillatory space in both the positive and negative directions. A choice either to the right or left of this optimum value will decrease the symmetrical output voltage swing capability of the amplifier. In Figure 5.43, the Q-point is chosen so that:

$$x = y.$$

Simple geometry applied to the Figure yields the expressions:

$$y = \left(\frac{m_{dc}}{m_{ac}}\right)[S - Q] \qquad \text{and} \qquad x = Q - C. \tag{5.196}$$

Solving for the Q-point yields:

$$\left(\frac{m_{dc}}{m_{ac}}\right)[S - Q] = Q - C \tag{5.197}$$

$$Q\left[1 + \left(\frac{m_{dc}}{m_{ac}}\right)\right] = \left(\frac{m_{dc}}{m_{ac}}\right)S + C. \tag{5.198}$$

The Quiescent point for maximum symmetrical swing is then determined to be:

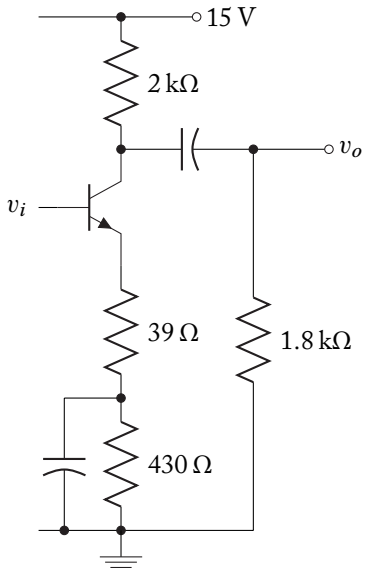
$$Q = \frac{\left(\frac{m_{dc}}{m_{ac}}\right)S + C}{1 + \left(\frac{m_{dc}}{m_{ac}}\right)}. \tag{5.199}$$

This optimum Q-point can easily be determined from only the ratio of the slopes of the AC and DC load lines and the limits on output voltage (the supply voltage and the minimum voltage edge of the linear region of the transistor).

Example 5.15

Design a resistor bias network that will achieve maximum symmetrical swing for the BJT output configuration shown. The Silicon BJT parameters are given as:

$$\beta_F = 150 \qquad V_A = 350.$$



Solution:

The output V-I relationship for BJTs is a plot of I_C vs. V_{CE}. The load lines must therefore express that relationship.

The expression for the DC load line is:

$$V_{CE} = 15 - I_C \left(2\,\text{k} + \frac{151}{150}469\right)$$

from which is determined:

$$m_{dc} = \frac{1}{\left(2\,\text{k} + \frac{151}{150}469\right)} = 0.4045{\times}10^{-3}.$$

The voltage limits on V_{CE} are given by:

$$S = 15V \qquad C = V_{CE(sat)} = 0.2\,\text{V}.$$

The AC load line slope is given by:

$$m_{ac} = \frac{1}{\frac{151}{150}39 + 2\,\text{k}//1.8\,\text{k}} = 1.0136{\times}10^{-3}.$$

The Q-point can then be calculated as:

$$Q = V_{CEQ} = \frac{\left(\frac{.4045}{1.0136}\right) 15 + 0.2}{1 + \left(\frac{.4045}{1.0136}\right)} = 4.42\,\text{V}.$$

With a quiescent collector current:

$$I_{CQ} = 4.279 \text{ mA}.$$

The collector-emitter voltage will vary from approximately 0.2 V to 8.64 V with a symmetrical excursion of 4.22 V about a quiescent value of 4.42 V.

The most obvious resistor bias scheme is the self-bias circuit. The base of the BJT must be at

$$V_{BQ} = -I_{EQ}\,(469) + 0.7 = 2.72\,\text{V}.$$

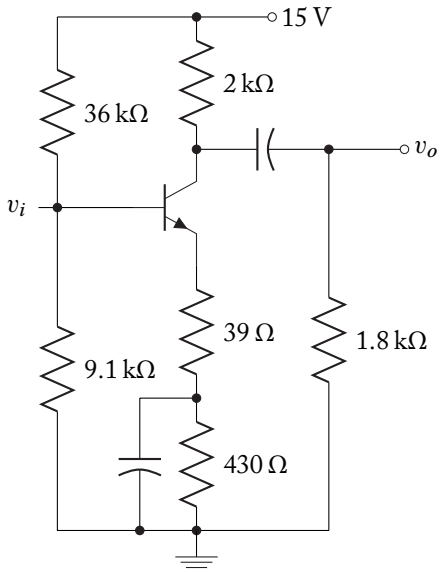
Without any restrictions on the input resistance of the amplifier, a wide variety of resistor pair values will achieve proper biasing. A common rule of thumb for bias stability is the current through the base bias resistors should be at least ten times the BJT base current. Using that rule, the maximum resistance that can be connected between the base and ground is:

$$R_{b2(\max)} = \frac{2.72}{10\ (4.279\text{m}/150)} = 9.53\,\text{k}\Omega.$$

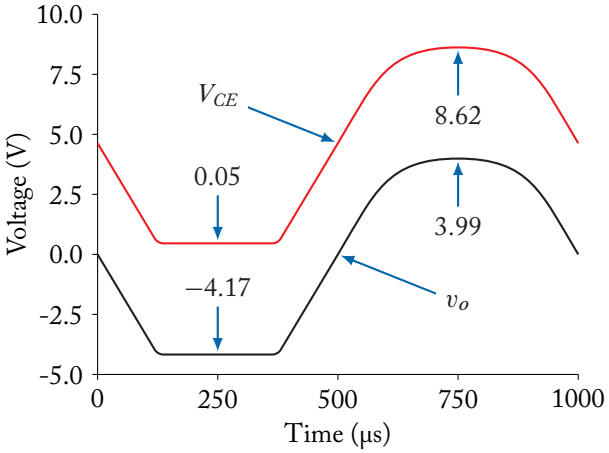
The closest 5% standard resistor value is 9.1 kΩ. Thus, choose $R_{b2} = 9.1\,\text{k}\Omega$. The value of the resistor between the power supply and the BJT base is given by:

$$R_{b1} = \frac{15 - 2.72}{\left(\frac{4.279\,\text{m}}{150}\right) + \left(\frac{2.72}{9.1\,\text{k}}\right)} = 37.5\,\text{k}.$$

The nearest 5% standard resistor value to this optimum value is 36 kΩ. It will provide proper operation within acceptable production standards. The final circuit topology is given by the figure on the right.



A SPICE simulation of the maximum symmetrical swing properties of both V_{CE} and v_o for this circuit follows. The rounding of resistor values and the fact that the simulation value of $V_{CE(sat)} = 0.05$ V rather than 0.2 V as used in calculations has introduced a slight deviation in both the Q-point and the swing. Distortion is the cause of dissimilar shaped limiting of the signal at the two ends.



5.13 CONCLUDING REMARKS

The small-signal model of the BJT was developed in this chapter using two-port network analysis and the Ebers-Moll transistor model. Three configurations of BJT amplifiers were described: common-emitter, common-collector, and common-base. The current gain, input resistance, output resistance, and voltage gain o feach of the configurations were found.

The FET small-signal model was also developed three configurations of FET amplifiers were described: common-source, common-drain, and common-gate. The input resistance, voltage gain, and output resistance were found for each configuration.

The modeling process for transistor circuit performance contains the following steps:

1. Determine the quiescent (DC) conditions. Verify that the BJT is in the forward-active region or the FET is in the saturation region.

2. Determine the transistor small-signal parameters from the quiescent conditions.

3. Create the AC equivalent circuit.

4. Determine the AC performance by replacing the transistor by its small-signal model.

5. Add the results of the CD and AC analysis to obtain total circuit performance.

Restrictions on amplification were shown to be dependent on transistor quiescent conditions. A technique that analytically determines the Q_point for maximum symmetrical swing based on load lines was introduced.

Summary Design Example

Whenever the physical distance between a signal source and the load are more than a very small fraction of a wavelength, the wires connecting the source and load appear to act as a transmission line. The voltage and current waveforms traveling on a transmission have amplitudes related by the *characteristic impedance* of the transmission line, Z_o. This characteristic impedance is a function of the geometry of the transmission line and the dielectric material surrounding the line.

The interfaces between the source, transmission line, and the load must be carefully controlled in order to avoid signal reflections: signal reflections produce an "echo" effect. In order to ensure that there are no signal reflections at the source end or the load end of the transmission line, the output resistance of the source and the input resistance of the load must be equal to the characteristic impedance of the transmission line.

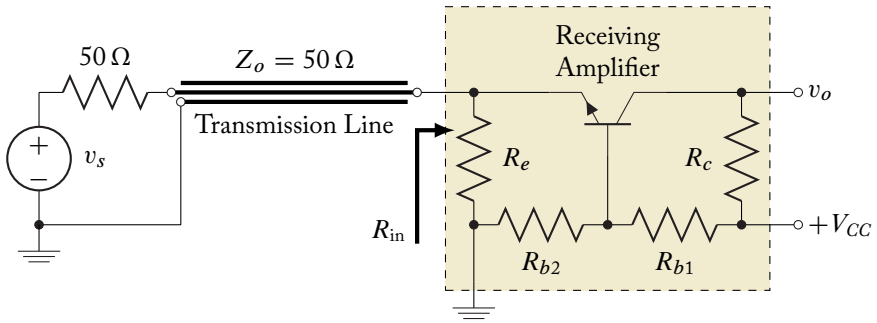
Design an amplifier that will accept an input signal from a matched 50 Ω transmission line system. The amplifier will have a voltage gain of ±10.

Solution:

In order to have no reflections at the load, the input resistance of the amplifier must be 50 Ω. The only amplifier topologies that have small input resistance while maintaining a voltage gain are the common-base and common-gate configurations. Of these two, the common-base configuration is much more common: the common-base configuration is chosen for this design. Assume typical transistor parameters:

$$\beta_F = 150, \qquad V_A = 160.$$

The basic topology of the common-base receiving circuit is shown below. Note that the source is an AC source with an output resistance matched to the characteristic impedance of the transmission line.



The expressions for the input resistance and voltage gain of a common-base amplifier are found in Table 5.5:

$$R_i = \frac{h_{ie} + R_b}{h_{fe} + 1} \quad \text{and} \quad A_V = \frac{h_{fe} R_c}{h_{ie} + R_b}.$$

The design requirement for a 50 Ω implies that:

$$R_{in} = R_e // R_i = R_e // \frac{h_{ie} + R_b}{h_{fe} + 1}$$

$$50 = R_e // \frac{h_{ie} + R_b}{h_{fe} + 1} = R_e // \frac{(h_{fe} + 1)\,\dfrac{\eta\, V_t}{I_c} + R_b}{h_{fe} + 1} = R_e // \left[\frac{\eta V_t}{I_c} + \frac{R_b}{h_{fe} + 1}\right].$$

The choice of R_c is somewhat arbitrary: 50 Ω is the lower limit with large values limiting the symmetrical swing of the amplifier. Choose $R_e = 100\,\Omega$. The quiescent collector current can also be somewhat arbitrarily chosen (the input resistance requirement and the previous choice of R_c place a lower limit of 0.26 mA on I_c).

Choose $I_c = 2\,\text{mA}$. This choice constrains R_b:

$$50 = 100 // \left[\frac{26\ \text{mV}}{2\ \text{mA}} + \frac{R_b}{151}\right] \qquad \Rightarrow \qquad R_b = 13.137\ \text{k}\Omega.$$

With this bias condition the h-parameters of the BJT are given by:

$$h_{fe} = \beta_F = 150 \qquad h_{ie} = (\beta_F + 1)\frac{\eta V_t}{I_c} = 151(13) = 1.963\,\text{k}\Omega$$

$$h_{oe}^{-1} = \frac{V_A}{I_c} = \frac{160\ \text{V}}{2\ \text{mA}} = 80\ \text{k}\Omega.$$

The design requeriment for a gain of 10 yields the value of the collector resistor:

$$10 = \frac{h_{fe} R_c}{h_{ie} + R_c} = \frac{150 R_c}{15.1\ \text{k}\Omega} \quad \Rightarrow \quad R_c = 1.007\ \text{k}\Omega \approx 1.01\,\text{k} \quad \text{(standard value)}.$$

For DC conditions, the transmission line acts as a short circuit. Thus, the effective emitter resistor is the parallel combination of the source output resistance and R_e:

$$R_{e(eff)} = 50 // R_e = 33.33\,\Omega.$$

In order to achieve maximum output swing the power supply must be chosen so that the maximum collector current is double the quiescent collector current:

$$V_{CC} > 4\,\text{mA}\ (R_{e(eff)} + R_c) = 4.173\,\text{V}.$$

Choose $V_{CC} = 5\,\text{V}$.

The only unknown component values are the base resistors R_{b1} and R_{b2}. These are determined in the usual fashion:

$$\frac{R_{b1}R_{b2}}{R_{b1}+R_{b2}} = R_b = 13.137\ \text{k}\Omega$$

and

$$\frac{R_{b2}}{R_{b1}+R_{b2}}5 = V_{bb} = \frac{(\beta_F+1)I_c}{\beta_F}R_{e(eff)} + 0.7 + \frac{R_b I_c}{\beta_F+1} = 0.94023\ \text{V}.$$

Dividing the upper equation by the lower equation results in:

$$\frac{R_{b1}}{5\ \text{V}} = \frac{13.137\ \text{k}\Omega}{0.94013\ \text{V}} \quad \Rightarrow \quad R_{b1} = 69.87\ \text{k}\Omega \approx 69.8\ \text{k}\Omega \quad \text{(standard value)}$$

and

$$R_{b2} = \left[\frac{1}{R_b} - \frac{1}{R_{b1}}\right]^{-1} = 16.18\ \text{k}\Omega \approx 16.2\ \text{k}\Omega \quad \text{(standard value)}.$$

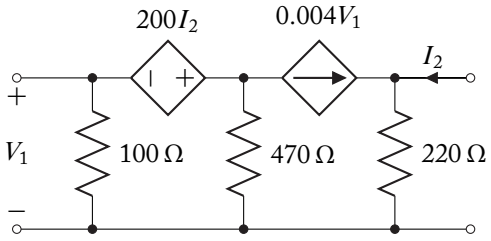
Commponent Summary:

Common-base amplifier: BJT parameters: $\beta_F = 150$, $V_A = 160\,\text{V}$.

$$R_{b1} = 69.8\,\text{k}\Omega \qquad R_{b2} = 16.2\,\text{k}\Omega.$$
$$R_c = 1.01\,\text{k}\Omega \qquad R_e = 100\,\Omega \qquad V_{CC} = 5\,\text{V}.$$

5.14 PROBLEMS

5.1. Determine the h-parameters for the given two-port network.



5.2. A two port network has the following y-parameters:

$$y_{11} = 0.03\,\text{S} \quad y_{12} = 0.00001\,\text{S}$$
$$y_{21} = 0.05\,\text{S} \quad y_{22} = 0.02\,\text{S}.$$

Determine the equivalent circuit representation of the two port network.

5.3. The h-parameter representation for a BJT in a particular common-emitter application is:

$$h_{ie} = 1.2\,\text{k}\Omega \quad h_{re} = 0.1\,\text{mV/V}$$
$$h_{fe} = 150 \quad\quad h_{oe} = 10\,\mu\text{S}.$$

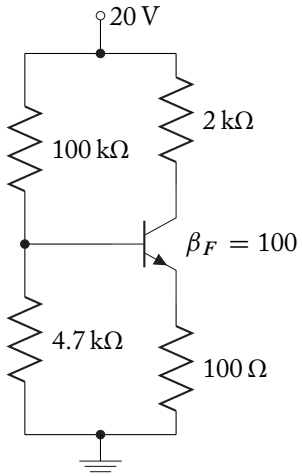
Determine the equivalent BJT g-parameters for this application.

5.4. A Silicon BJT is described by $\beta_F = 160$ and $V_A = 120\,\text{V}$. Determine h_{ie}, h_{fe}, and h_{oe} for the following quiescent conditions:

(a) $I_c = 2\,\text{mA}$

(b) $I_c = 0.5\,\text{mA}$

5.5. Determine the significant BJT h-parameters when operating in the given circuit.



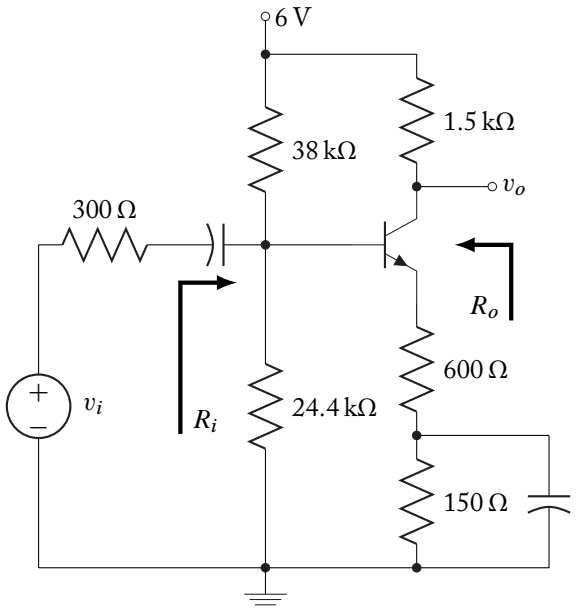
5.6. A transistor with $\beta_F = 200$ is used in the circuit shown. Assume the capacitors are infinite.

(a) Determine the quiescent conditions for the transistor.

(b) Determine the BJT h-parameters.

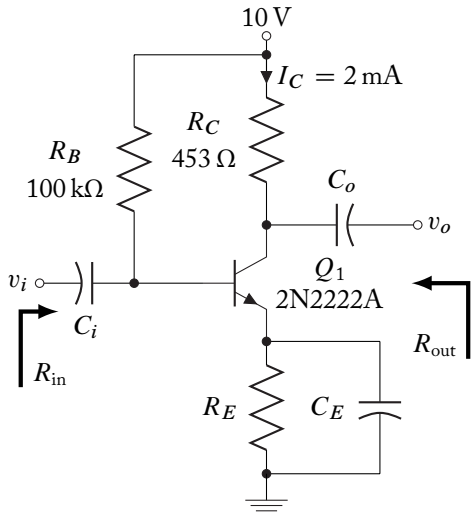
(c) Determine the AC circuit parameters:

$A_v = v_o/v_i$
R_i, as shown
R_o, as shown.



5.7. Complete the design by finding the value for R_E to establish the given quiescent conditions. Draw the midband small signal equivalent circuit for the circuit below. Determine the appropriate h-parameters for the model and find midband input resistance R_{in}, output resistance R_{out}, and voltage gain of the circuit.

Assume that $V_{BE} = 0.7\,\text{V}$ and $\beta_F = 200$.



5.8. For the common-collector circuit shown, assume a Silicon BJT with $\beta_F = 75$.

(a) Determine the value of R_B so that $I_C = 7\,\text{mA}$

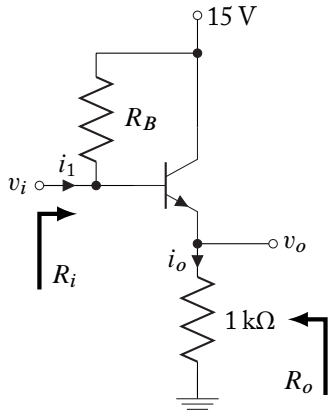
(b) Determine the amplifier performance parameters

$A_I = i_o/i_i$

$A_v = v_o/v_i$

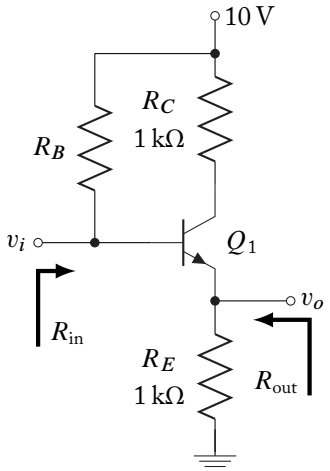
R_i, as shown

R_o, as shown.

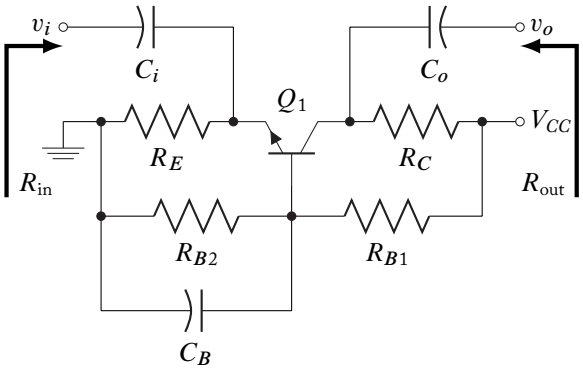


5.9. Complete the design by finding the value for R_B so that the quiescent $I_C = 2\,\text{mA}$. Determine the quiescent voltages and currents. Draw the midband small-signal equivalent circuit for the circuit below, and determine the midband input resistance R_{in}, output resistance R_{out}, and voltage gain of the circuit.

Assume that $V_{BEQ} = 0.7\,\text{V}$ and $\beta_F = 180$.

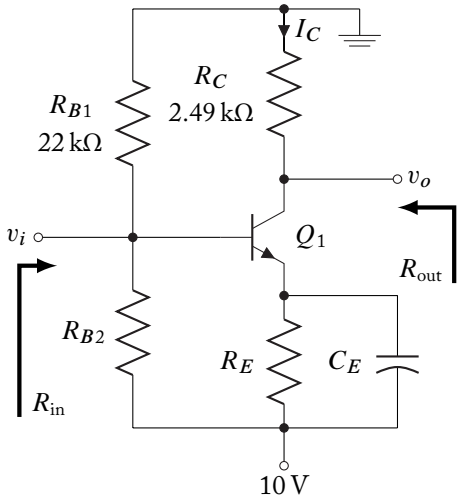


5.10. Draw the midband small-signal equivalent circuit for the circuit below. Find the expressions for the midband input resistance R_{in}, output resistance R_{out}, and voltage gain of the circuit.

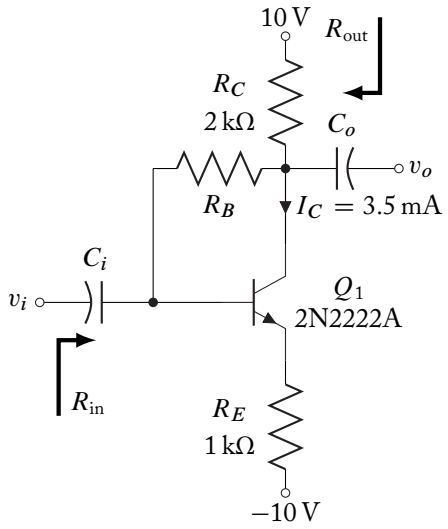


5.11. Complete the design of the circuit below for $R_{in} = 1.5\,\text{k}\Omega$ and determine the quiescent currents and voltages. Draw the midband small signal equivalent circuit. Determine the appropriate h-parameters for the small signal model and find the midband voltage gain, input resistance R_{in}, and output resistance R_{out}. Assume that

$$V_{BEQ} = 0.7\,\text{V},\ \beta_F = 150,\ I_C = -2\,\text{mA}.$$



5.12. Complete the design of the circuit below and draw the midband small signal equivalent circuit. Determine the quiescent currents and voltages. Draw the small signal equivalent circuit. Determine the appropriate h-parameters for the small signal model and find the midband voltage gain, input resistance R_{in}, and output resistance R_{out}.



5.13. For the circuit shown:

(a) Find the quiescent currents and voltages.

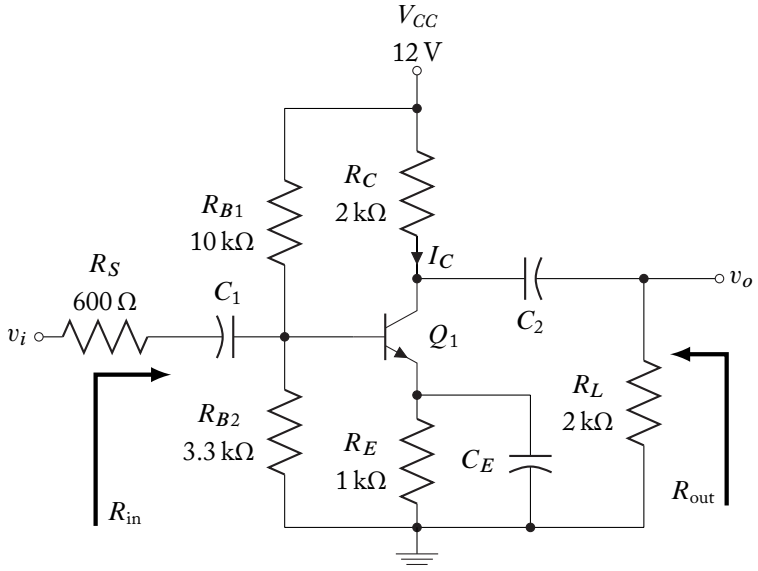
(b) The overall midband voltage gain A_{vs}, R_{in}, and R_{out}.

(c) The maximum symmetrical swing and corresponding maximum peak-to-peak input signal.

Assume the following transistor parameters:

$$\beta_F = 220,\ V_{BE} = 0.7\,\text{V}.$$

All capacitors are sufficiently large to have small reactances.



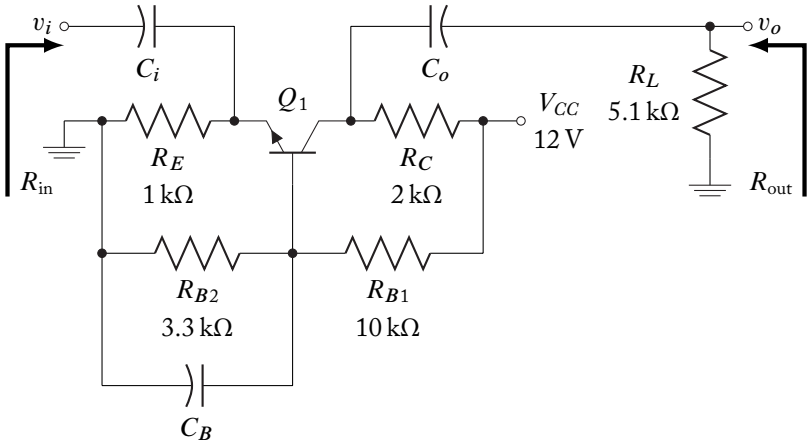
5.14. For the circuit shown:

(a) Find the quiescent currents and voltages.

(b) Determine the overall midband voltage gain, A_{vs}, and the input and output resistances, R_{in}, and R_{out}.

(c) The maximum symmetrical output voltage swing and corresponding maximum peak-to-peak input signal.

Assume the following transistor parameters in SPICE: BF = 180, VA = 100, IS = 6.8 F.



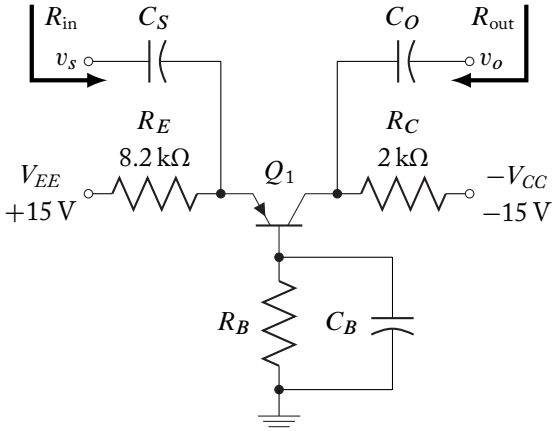
5.15. For the amplifier circuit shown:

(a) Complete the design of the common-base BJT amplifier shown below for a bias stability of 1% change in I_C for a 10% change in β_F. The *pnp* transistor parameters are:

$$V_A = 150\,\text{V} \quad \text{and} \quad \beta_F = 120.$$

(b) Determine the midband voltage gain of the amplifier.

(c) Find the input resistance, R_{in}, and output resistance, R_{out}.

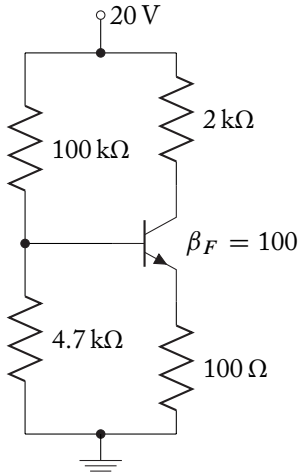


5.16. Design a non-inverting amplifier with a gain of $10 < A_v < 25$ with an input resistance of 50 Ω ± 20% and an output resistance of 600 Ω ± 20%. Use a 2N3906 *pnp* BJT with the characteristic curves found in the appendix. Determine the maximum undistorted output signal for the design and the corresponding input signal. Available power supply voltages: ±12 V.

5.17. An amplifier with low input resistance and moderate voltage gain is to be developed from the self-bias circuit shown.

(a) Indicate the proper input and output terminals to meet the design goals. Insert appropriate bypass capacitors to improve the performance characteristics.

(b) Determine the voltage gain and input resistance of the design.



5.18. Design an impedance buffer/transformer using a 2N2222 *npn* BJT. The specifications for the buffer/transformer are:

Input resistance:	$12\,\text{k}\Omega \pm 20\%$
Output resistance:	$51\,\Omega \pm 20\%$
Available power supply voltages:	$\pm 12\,\text{V}$.

Determine the voltage and current gains of the circuit.

5.19. The amplifier shown was *supposed* to have been designed for a voltage gain

$$A_{vs} = -33 \pm 20\%.$$

However, its output is $v_o = 0$ for all input voltages v_i. Something is wrong with this amplifier. The transistor parameters are:

$$\beta_F = 180,\ V_{BE} = 0.7\,\text{V}.$$

All capacitors are sufficiently large to have small reactances.

(a) Why doesn't the amplifier work properly?

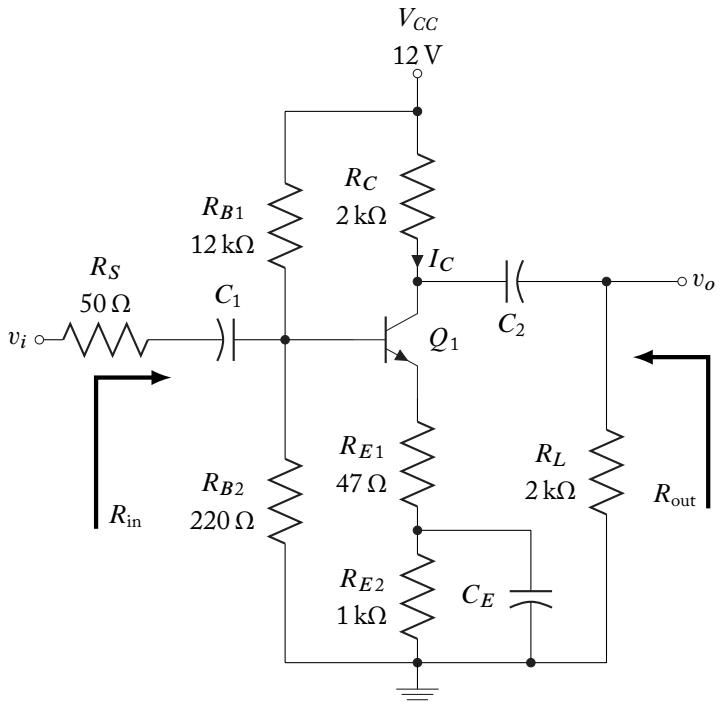
(b) Re-design the bias network for the new quiescent conditions by solving for I_C from h_{ie} using the small-signal model with

$$A_{vs} = \frac{v_o}{v_s} = -33.$$

There is no specification on R_{in}.

(c) Determine A_{vs}, R_{in}, and R_{out}.

(d) Determine the maximum symmetrical output voltage swing and corresponding maximum peak-to-peak input signal.



5.20. Table 5.8 itemizes several alternate expressions for the determination of the mutual transconductance, g_m, for field effect transistors. Show the equivalence of the various forms for each type of FET.

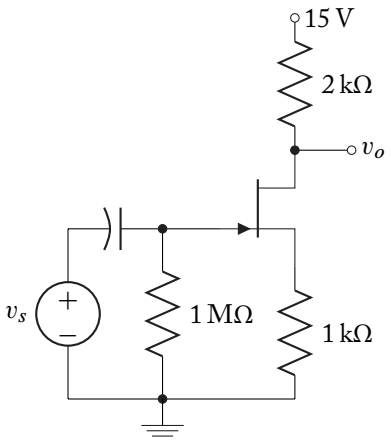
5.21. Given a JFET with parameters:

$$V_{PO} = -4\,\text{V}$$
$$I_{DSS} = 10\,\text{mA}$$
$$V_A = 120\,\text{V}$$

operating in the circuit shown.

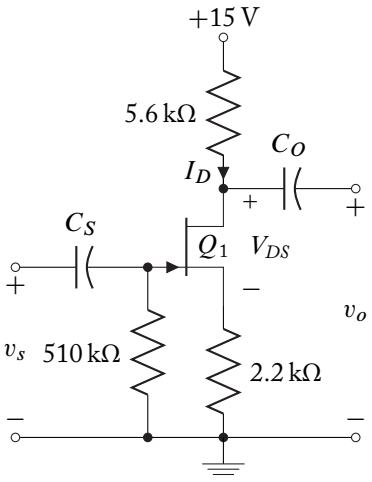
(a) Determine the FET small-signal parameters.

(b) Determine the amplifier small-signal performance characteristics in its midband frequency range.



5.22. Find the midband voltage gain for the circuit shown. The *n*-channel JFET parameters are:

$$I_{DSS} = 7\,\text{mA},\ V_{PO} = 4\,\text{V},\ \text{and}\ V_A = 120\,\text{V}.$$

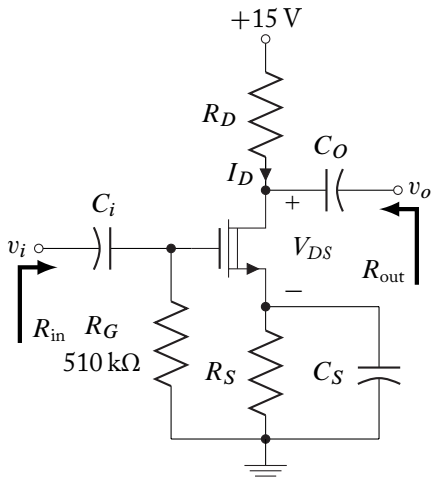


5.23. Complete the design of the *n*-channel depletion MOSFET circuit to achieve a Qpoint: $I_D = 1\,\text{mA}$, and $V_{DS} = 4\,\text{V}$.

Draw the midband small signal model and find midband input resistance R_{in}, output resistance R_{out}, and voltage gain of the amplifier.

The MOSFET parameters are:

$$V_A = 100\,\text{V},\ I_{DSS} = 8\,\text{mA}\ \text{and}\ V_{PO} = -2\,\text{V}.$$



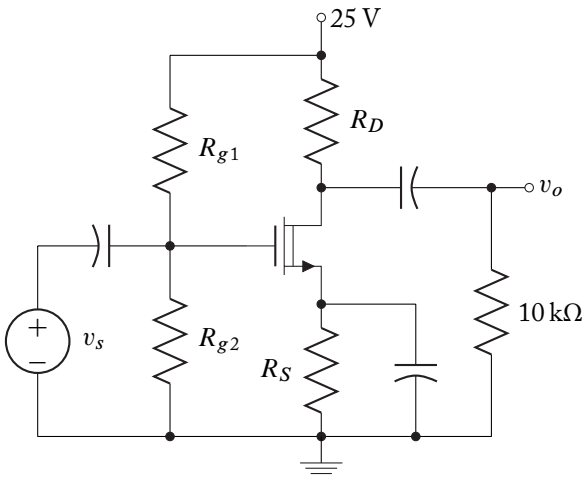
5.24. The MOSFET amplifier circuit shown is to be designed for a midband voltage gain of −8. The circuit is to be biased for the following quiescent condition:

$$I_D = 5\,\text{mA}$$
$$V_{DS} = 5\,\text{V}.$$

The transistor parameters are:

$$I_{DSS} = 8\,\text{mA}$$
$$V_{PO} = -3\,\text{V}$$
$$V_A = 60\,\text{V}.$$

Complete the design.



5.25. Complete the design of the MOSFET circuit shown so that

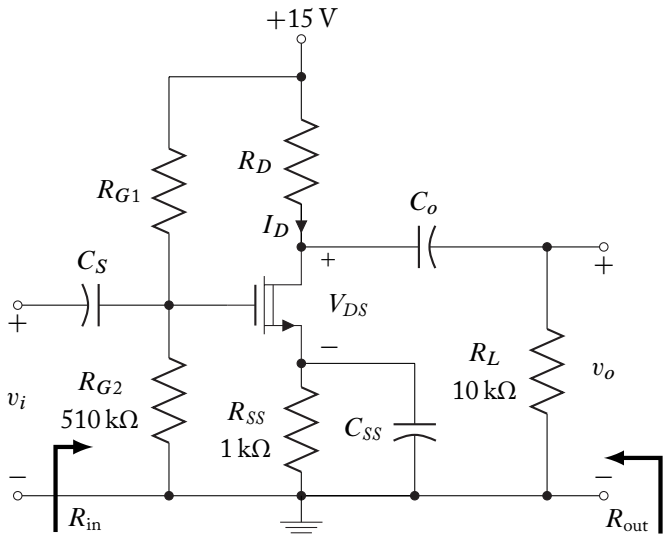
$$I_D = 4\,\text{mA} \quad \text{and} \quad V_{DS} = 5\,\text{V}.$$

The MOSFET parameters are:

$$I_{DSS} = 5\,\text{mA},\ V_{PO} = -3\,\text{V}$$
$$V_A = 100\,\text{V}.$$

Find the voltage gain, $A_{vs} = \frac{v_o}{v_i}$, R_{in}, and R_{out}.

Use SPICE to verify the DC conditions, midband voltage gain, R_{in}, and R_{out} of the amplifier. All capacitors are sufficiently large to have small reactances.



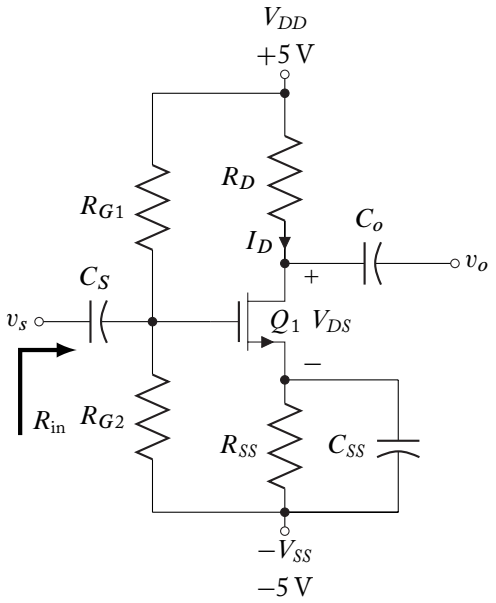
5.26. Complete the design of the amplifier shown to establish operation at $V_{GS} = V_{DS} = 2V_T$ with equal values of R_S and R_D. The input resistance, R_{in}, is 730 kΩ ± 5%. The n-channel enhancement MOSFET parameters are:

$$V_T = 1.5\,\text{V} \quad K = 0.5\,\text{mA/V}^2.$$
$$V_A = 100\,\text{V}.$$

(a) Find I_D and V_{DS}

(b) Find R_S, R_D, R_{G1}, and R_{G2}.

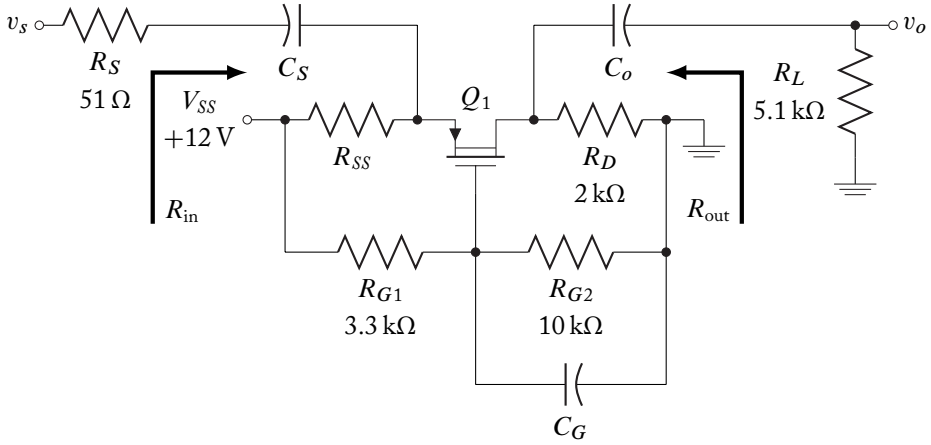
(c) Determine the midband voltage gain of the amplifier.



5.27. Complete the design of the common-gate amplifier so that $I_D = -1$ mA. Determine the quiescent voltages and currents, the voltage gain, $A_{vs} = \frac{v_o}{v_s}$, R_{in}, and R_{out}.

The FET parameters of interest are: $I_{DSS} = 6$ mA,

$$V_{PO} = 2.5\,\text{V}, \quad V_A = 100\,\text{V}.$$



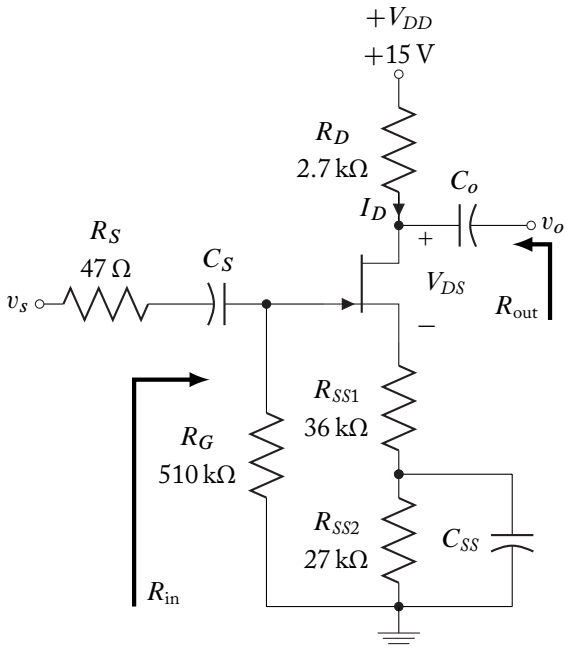
5.28. Design a non-inverting amplifier with midband voltage gain $A_{vs} \geq 2$ and output resistance, $R_{out} = 1\,\text{k}\Omega \pm 20\%$, input resistance, $R_{in} = 100\,\Omega \pm 25\,\Omega$ using the 2N5461 p-channel JFET. The 2N5461 specification sheet is found in the appendix. Use the typical

values of the parameters: that is, use the average of the maximum and minimum values, unless only maximum or minimum values are given. The Gate-Source Cutoff Voltage, $V_{GS(off)}$, specification is equivalent to FET pinch-off voltage, V_{PO}, and the Output Conductance, Re(V_{os}), specification is equivalent to g_d.

(a) What is the quiescent condition of the JFET?

(b) Confirm the design using SPICE.

5.29. The amplifier shown has, as its output, $v_o = 0$ for all input voltages v_i. Something is wrong with this amplifier. The 2N5484 transistor parameters are given on the specification sheet found in the appendices. Use the typical values of the parameters: that is, use the average of the maximum and minimum values, unless only maximum or minimum values are given. The Gate-Source Cutoff Voltage, $V_{GS(off)}$, specification is equivalent to FET pinchoff voltage, V_{PO}, and the Output Conductance, Re(V_{os}), specification is equivalent to g_d.



All capacitors are sufficiently large to have small reactances.

(a) Why doesn't the amplifier work properly?

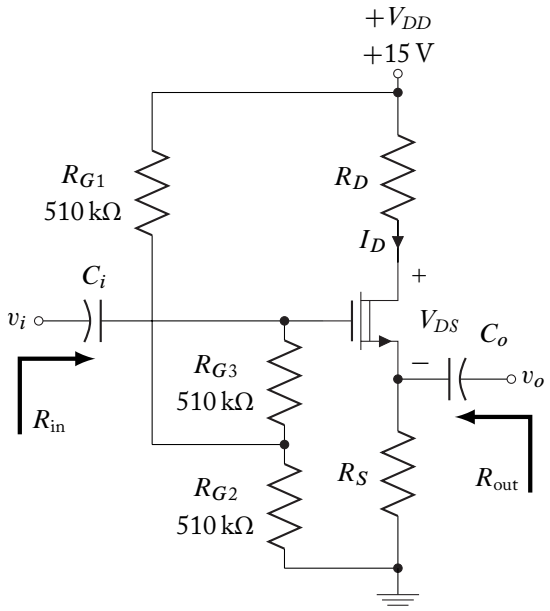
(b) Re-design the bias network for the new quiescent conditions of $I_D = 1$ mA and $V_{DS} = 4$ V.

(c) Determine A_{vs}, R_{in}, and R_{out}. Use SPICE to verify the DC conditions, midband voltage gain, R_{in}, and R_{out} of the amplifier.

(d) Determine the maximum symmetrical output voltage swing and corresponding maximum peak-to-peak input signal.

5.30. What is the midband voltage gain and output resistance of a common-drain amplifier when the output is taken from the source of the re-designed circuit in the previous problem? What are the new quiescent conditions, midband voltage gain, input resistance, and output resistance of the common-drain amplifier if $R_{SS1} = 2.7\,\text{k}\Omega$, $R_{SS2} = 0\,\Omega$, and C_{SS}?

5.31. Design a circuit to bias an n-channel depletion MOSFET described by: $V_A = 100\,\text{V}$, $I_{DSS} = 9\,\text{mA}$, and $V_{PO} = -3\,\text{V}$ using the "bootstrapping" configuration shown. The design specifications require that $I_D = 2\,\text{mA}$ and $V_{DS} = 3\,\text{V}$. The "bootstrapping" bias technique is used to preserve the high input resistance of the circuit. Draw the midband small signal model and find midband input resistance R_{in}, output resistance R_{out}, and voltage gain of the amplifier.



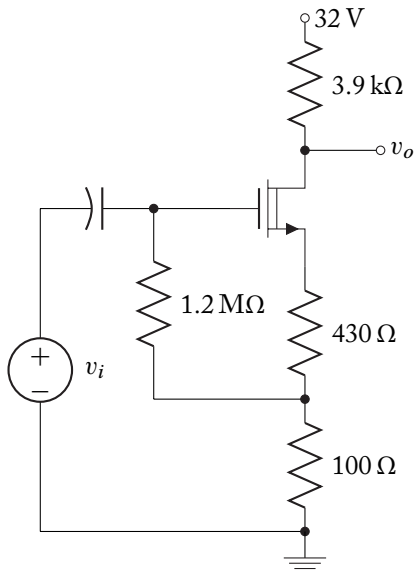
5.32. Assume an n-channel depletion type MOSFET with parameters:

$$I_{DSS} = 9\,\text{mA}$$
$$V_{PO} = -4.5\,\text{V}$$
$$V_A = 140\,\text{V}.$$

Determine the midband AC voltage gain,

$$A_v = \frac{v_o}{v_i}.$$

Note: this circuit is *not* one of the topology types for which simple AC parameter expressions have previously been determined. The gain must be derived from the AC transistor model inserted into the circuit.



5.33. The common-emitter amplifier with constant current source biasing shown does not meet the required design specifications. The specifications are:

Q_1 : $I_C = 2\,\text{mA}$, $V_{CE} = 3\,\text{V}$, for a power dissipation of 6 mW for the BJT.
$\beta_F = 220$
$V_{BE} = 0.7\,\text{V}$
Q_2 : $V_T = 2\,\text{V}$
$K = 500\,\mu\text{A/V}^2$.

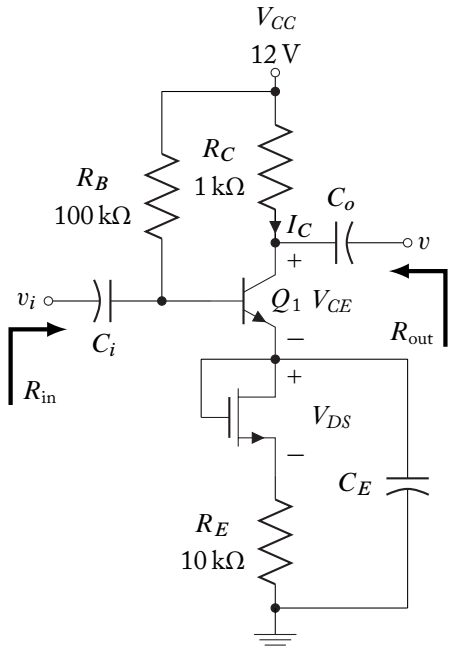
All capacitors are sufficiently large to have small reactances.

(a) Why does the circuit not meet specifications?

(b) Re-design the amplifier to meet the specifications.

(c) Find the voltage gain, and input and output resistances.

(d) Estimate the total power dissipated.



5.34. The common-collector buffer amplifier (using Q_1) shown does not meet the required design specifications. The FET Q_2 forms a constant current source. The specifications are: $I_C = 2\,\text{mA}$, Q_1 maximum DC power dissipation: 15 mW($P_D = I_C$, $V_{CE} \leq 15\,\text{mW}$).

The transistor parameters are:

$$Q_1: \quad \beta_F = 120,\ V_{BE} = -0.7\,\text{V}.$$
$$Q_2: \quad K = 500\,\mu\text{A/V}^2,\ V_T = -2\,\text{V}.$$

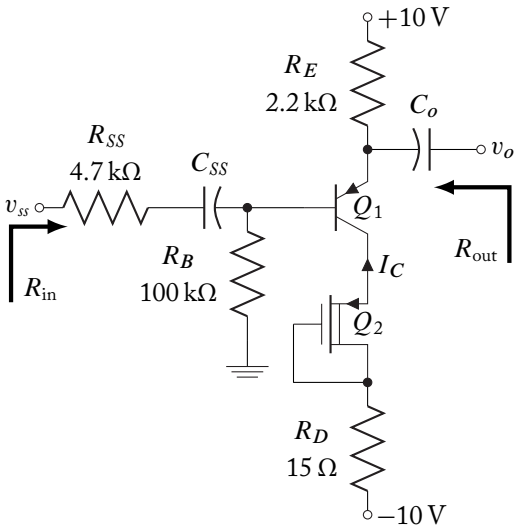
All capacitors are sufficiently large to have small reactances.

(a) Why does the circuit shown not meet the specifications?

(b) Re-design the bias network to fulfill the design specifications. Find the new quiescent currents and voltages V_{DSQ2}, I_{DQ2}, V_{GSQ2}, I_{CQ1}, V_{CEQ1}, and I_{BQ1}. (Hint: Design for $I_C = -2\,\text{mA}$ and $V_{EC} < 7.5\,\text{V}$, and alter R_D and R_B.)

(c) What is the total (DC) power dissipation?

(d) Determine the new overall midband voltage gain, $A_{vs} = \frac{v_o}{v_{ss}}$, R_{in}, and R_{out}.



5.35. Determine the proper connection for v_o, resistor values, and a power supply, V_{DD}, such that the following design goals are satisfied:

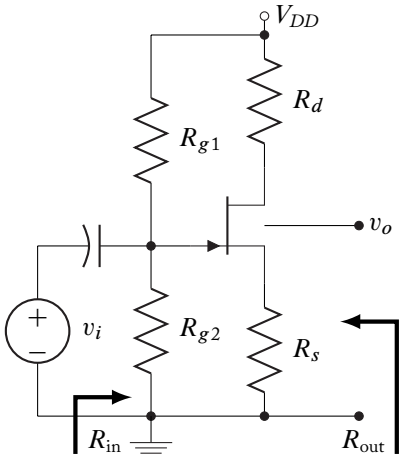
$$\left.\begin{aligned} R_{in} &= 50\ \text{k}\Omega \\ R_{out} &= 10\ \text{k}\Omega \end{aligned}\right\} \text{as shown on diagram.}$$

$$|A_v| = \left|\frac{v_o}{v_i}\right| = 7.0,$$

with quiescent drain current, $I_d = 2\,\text{mA}$.

Assume an n-channel JFET with:

$$I_{DSS} = 5\,\text{mA} \quad V_{PO} = -4\,\text{V} \quad V_A = -100\,\text{V}.$$



5.36. For the circuit shown, the BJT has parameters,

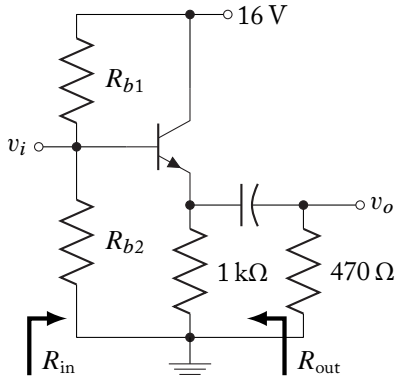
$$\beta_F = 150$$
$$V_A = 250\,\text{V}.$$

(a) Determine values of the unknown resistors such that maximum symmetrical swing of the output, v_o, will occur. It is required that the input resistance, $R_{in} \approx 24\,\text{k}\Omega$.

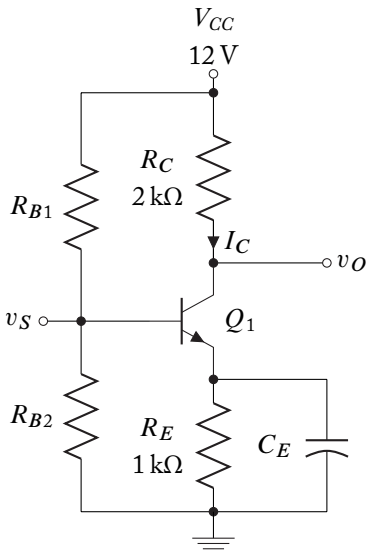
(b) Using the values found above, determine the voltage gain

$$A_v = \frac{v_o}{v_i},$$

and the output resistance R_{out}.



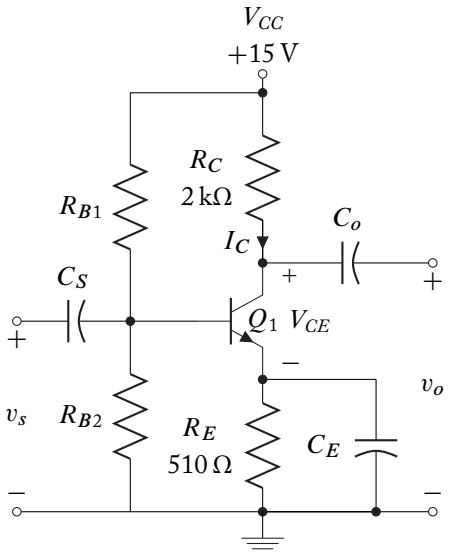
5.37. Complete the design of the circuit shown for maximum symmetrical collector current swing. Let $\beta_F = 180$, $V_\gamma = 0.7\,\text{V}$, use the "rule of thumb" relationship between R_E and R_B for stable operation (1% change in I_C for 10% change in β_F). Determine the quiescent conditions.



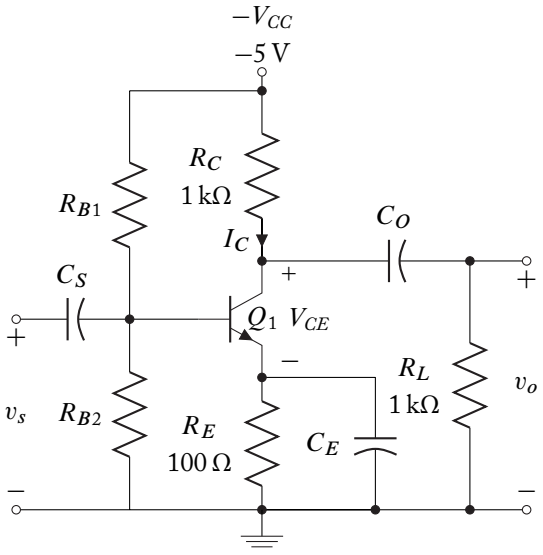
5.38. Design an inverting amplifier with a gain of $35 < |A_v| < 45$ with an input resistance of 12 kΩ ± 20% and an output resistance of 3.5 kΩ ± 20%. Use a 2N2222 BJT and design for maximum symmetrical swing. Available power supply voltages: +15 V.

How will the performance of the amplifier be altered if an emitter degenerative resistor (an emitter resistor that is not bypassed with a capacitor) of 51 Ω is used in the circuit?

5.39. Complete the design of the circuit shown for maximum symmetrical swing in the mid-band frequency range. The circuit is required to have a bias stability of 1% change in I_C for a 10% change in β_F. The transistor has a $\beta_F = 180$ and $V_A = 200$ V.



5.40. Complete the design of the circuit shown for maximum symmetrical swing in the midband frequency range. The circuit is required to be have a bias stability of 1% change in I_C for a 10% change in β_F. The *pnp* BJT has a $\beta_F = 120$ and $V_A = 120$ V.

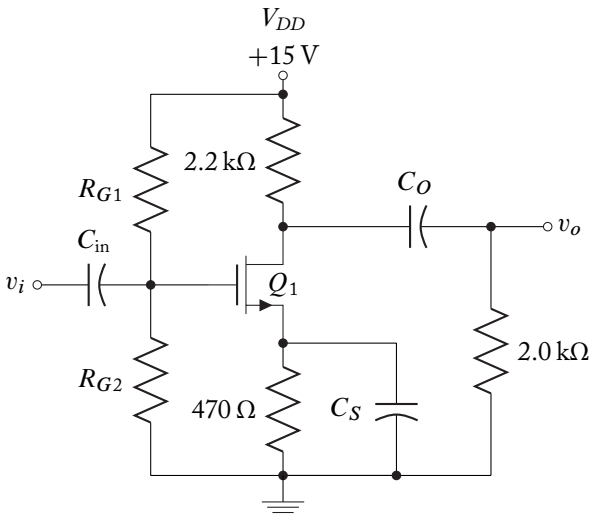


5.41. Designing for maximum symmetrical swing using FETs is challenging due to the dependence of the minimum linear voltage on quiescent conditions. For a FET this voltage

occurs at the transition between the ohmic and saturation regions. For the circuit application shown, complete the design so that maximum symmetrical swing is achieved. Explain your methodology for determining the Q-point.

The FET is described by:

$$K = 1\,\text{mA/V}^2$$
$$V_{TO} = 1.2\,\text{V}$$
$$V_A = 110\,\text{V}.$$



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CHAPTER 6

Multiple-Transistor Amplifiers

Previous discussions of transistor amplifiers have shown that single transistor amplifiers have a wide range of possible design characteristics described by the principal performance characteristics: voltage and current gain; input and output resistance. There are, however, many circumstances when the desired overall performance characteristics for an amplifier cannot be met by a single transistor amplifier. That is, the required combination of amplification, input resistance, and output resistance may be beyond the capability of a single transistor amplifier. In these circumstances it is necessary to employ amplifiers that use more than a single transistor.

The obvious approach to changing amplifier performance characteristics is to cascade (connect the output of a given stage directly into the input of the following stage) single transistor amplifiers. In this manner, additional gain or the modification of input/output resistance can be easily accomplished. This simple approach to multiple transistor amplifiers is discussed in Section 6.1. A major drawback to this approach is the relatively high number of electronic components necessary to accomplish a design. In addition, if the simple stage are coupled with capacitors (a common practice to decouple the DC bias conditions of each stage), the low frequency performance of the amplifier can be severely degraded.

Several transistor cascades are commonly packaged as a single unit. Most common among these cascade types are the Darlington configurations. These cascade configurations have the advantage of simple external bias circuitry, high performance, and DC coupling of stages. Analysis of these types is discussed in Section 6.2.

Differential amplifiers are another type of high-performance multiple transistor amplifier. They commonly are based on the high gain of emitter-coupled and source-coupled transistor amplifiers. Operational amplifiers are a common form of differential amplifier that typically have emitter-coupled or source-coupled amplifiers as input stages.

In addition, the practice of biasing transistor amplifiers with transistor current sources will be explored in this Chapter. This bias technique is particularly suited to integrated amplifiers contained on a single semiconductor chip where transistors are more practical and economic devices than resistors.

Active (as opposed to resistive) loads will be explored as a means of increasing gain and modifying output resistance without the use of extremely large resistors and power supplies.

6.1 MULTISTAGE AMPS USING SIMPLE STAGES CASCADED

Among the many multistage connections possible in large amplifiers, the cascade connection is the most simple. In a cascade connection, the output voltage and current of an amplifier stage are passed directly to the input of the next amplifier stage. A two-stage cascade-connected amplifier is represented by Figure 6.1. In this amplifier, the outputs, v_{o1} and i_{o1}, of the first amplifier stage become the inputs, v_{i2} and i_{i2}, to the second stage without any modification. For the discussions in this section, it is assumed that each of the amplifier stages consists of one of the simple single-transistor amplifiers described in Chapter 5.[1]

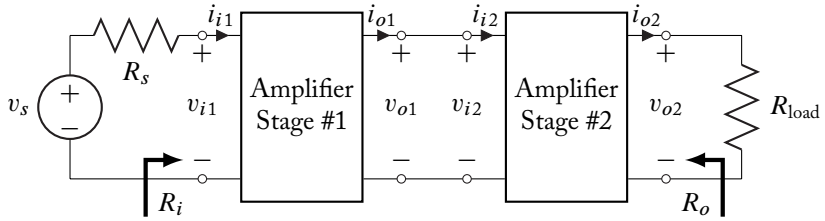


Figure 6.1: An amplifier consisting of two cascaded stages.

The advantage of cascade-connected amplifiers becomes apparent in the analysis procedure. The overall voltage gain, for example, of the amplifier of Figure 6.1 is given by the ratio of the load voltage to the source voltage:

$$A_V = \frac{v_{o2}}{v_s}. \tag{6.1}$$

A simple progression through the stages of the amplifier expands this expression to more familiar expressions:

$$A_V = \frac{v_{o2}}{v_s} = \left(\frac{v_{o2}}{v_{i2}}\right)\left(\frac{v_{i2}}{v_{o1}}\right)\left(\frac{v_{o1}}{v_{i1}}\right)\left(\frac{v_{i1}}{v_s}\right) = (A_{V2})\,(1)\,(A_{V1})\left(\frac{R_i}{R_i + R_s}\right), \tag{6.2}$$

where

A_{V1} = the voltage gain of the first amplifier stage, and
A_{V2} = the voltage gain of the second amplifier stage.

The total voltage gain of a cascade-connected amplifier can be expressed as a product of the gains of the individual stages and simple voltage divisions. The beauty of cascade-connected amplifiers comes in the second of the multiplicative terms of Equation (6.2): it is an expression of identity, and consequently can be eliminated from consideration. The expressions for the gains of the individual stages were developed in Chapter 5 and may be used directly in calculating the overall

[1]More complicated individual stages may be cascade-connected. The restriction of individual stages to simple single-transistor is for demonstration purposes only: later sections will include more complicated stages that are cascade-connected.

gain. It is, however, important to note that *each stage presents a load to the previous stage*: its input resistance is part of the total load that is apparent to a previous stage. In a similar fashion the current gain of a cascade-connected amplifier is the product of the current gains of the individual stages and simple current divisions. Again the individual stages interact, and the expressions for current gain must include the effects of that interaction. Total input resistance, R_i, or total output resistance, R_o, may also be modified by the interaction of individual stages.

Example 6.1

The two-stage cascade-connected amplifier shown is comprised of two identical amplifier stages. The two Silicon BJTs have characteristic parameters:

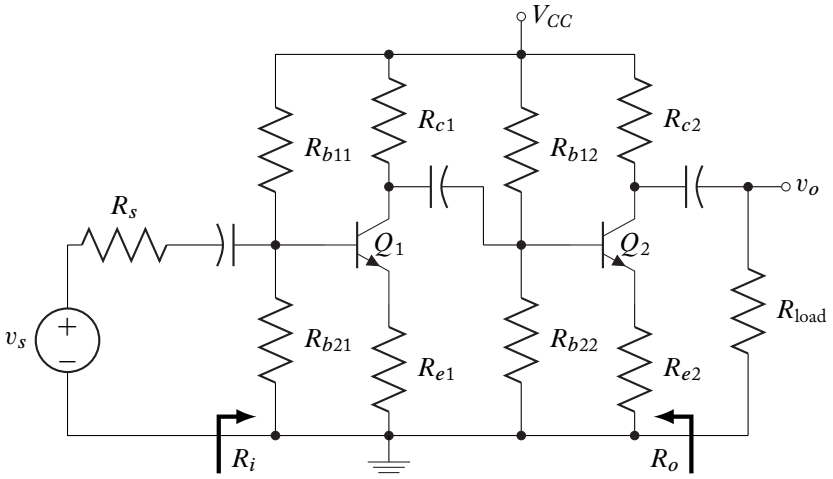
$$\beta_F = 150 \qquad V_A = 350.$$

The circuit resistors are given as:

$$\begin{aligned} R_{b11} &= R_{b12} = 82\,\text{k}\Omega & R_{c1} &= R_{c2} = 2.2\,\text{k}\Omega \\ R_{b21} &= R_{b22} = 12\,\text{k}\Omega & R_{e1} &= R_{e2} = 430\,\Omega \\ R_s &= 100 & R_{load} &= 2.7\,\text{k}\Omega\,. \end{aligned}$$

The power supply voltage is: $V_{CC} = 15\,\text{V}$.

Determine the AC voltage and current gain (from the source to the load) and the input and output resistances (as shown) for this amplifier.



Solution:

The determination of the performance of multistage amplifiers follows the same basic steps that were derived in Chapter 5:

1 Model the transistors with an appropriate DC model (circuit or analytic).

2 Determine the circuit quiescent (DC) conditions - verify active region for BJTs or saturation region for FETs.

3 Determine the transistor AC model parameters from the quiescent conditions.

4 Create an AC equivalent circuit.

5 Determine the AC performance of each amplifier stage by:

(a) replacing the transistors by their respective AC models, or

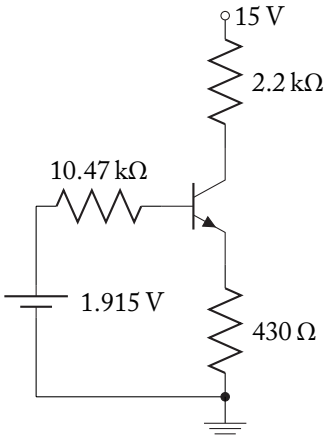
(b) using previously derived results for the circuit topology.

5a Combine the stage performance quantities to obtain total amplifier performance.

6 Add the results of the DC and AC analysis to obtain total circuit performance.

Only the fifth step has been modified to reflect the new condition that several stages may comprise the total amplifier.

Beginning with the amplifier stage containing Q1, the DC equivalent circuit, after replacing the base circuit with its Thévenin equivalent as is shown:



The base and collector currents are calculated to be:

$$I_B = \frac{1.915 - 0.7}{10.47\,\text{k} + 151\,(430)} = 16.11\ \mu\,\text{A}$$

and

$$I_C = 150\ I_B = 2.417\,\text{mA}.$$

V_{CE} must be checked to verify that the BJT is in the forward-active region:

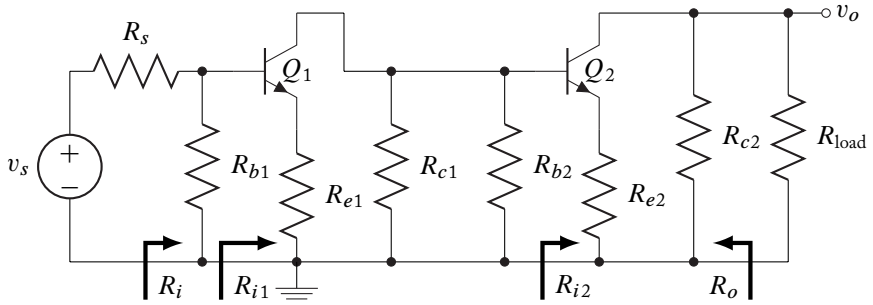
$$V_{CE} = 15 - I_C\,(2.2\text{k}) - \frac{151}{150} I_C\,(430) = 8.64\text{ V} \geq 0.2\text{ V}.$$

After verification, the BJT h-parameters can be determined:

$$h_{fe} = 150, \quad h_{ie} = 151\,\frac{\eta\, V_t}{|I_C|} = 1.624\text{ k}\Omega \quad \text{and} \quad h_{oe} = \left|\frac{I_C}{V_A}\right| = \frac{1}{144.8\text{ k}\Omega}.$$

In this amplifier the two stages are identically biased. Consequently, the BJT quiescent conditions in each amplifier stage and the resultant BJT h-parameters are the same. When the stages are *not* identical, the bias conditions and transistor parameters must be obtained for each stage.

The AC equivalent circuit for the two-stage amplifier is shown below:



where

$$R_{b1} = R_{b11}//R_{b21} = 10.47\,\text{k}\Omega, \text{ and } R_{b2} = R_{b12}//R_{b22} = 10.47\,\text{k}\Omega.$$

This AC model depicts a cascade-connected amplifier consisting of two common-emitter with emitter-resistor amplifier stages. The performance characteristics for simple BJT amplifier stages is given in Table 5.7: the characteristics will be reproduced here.[2] The input resistance of a $CE + R_e$ amplifier stage is:

$$R_i = h_{ie} + (h_{fe} + 1)R_e.$$

Since the stages are identical ($R_{e1} = R_{e2}$):

$$R_{i1} = R_{i2} = 1.624\,\text{k} + (151)430 = 66.55\,\text{k}\Omega.$$

The total amplifier input resistance is the parallel combination of the first stage bias resistors and input resistance:

$$R_i = R_{b1}//R_{i1} = 10.47\,\text{k}//66.55\,\text{k} = 9.0467\,\text{k}\Omega \approx 9.05\,\text{k}\Omega.$$

[2]The BJT parameter $1/h_{oe}$ is sufficiently large in comparison to the other circuit resistances that it has been ignored in all calculations.

The total amplifier output resistance is the output resistance of the second stage:

$$R_o = R_{o2} \approx R_{c2} = 2.2\,\text{k}\Omega.$$

The voltage gain for a $CE + R_e$ amplifier is:

$$A_V = \frac{-h_{fe} R_c}{h_{ie} + (h_{fe} + 1) R_e} = \frac{-h_{fe} R_c}{R_i}.$$

The only quantity yet undetermined in this gain expression is R_c, the total resistance connected to the collector terminal of the amplifier stage BJT. For the first amplifier stage, R_c is the parallel combination of R_{b2}, R_{c1}, and the input resistance to the second stage, R_{i2}. For the second stage, R_c is the parallel combination of R_{c2} and R_{load}. Notice that even though the amplifier stages are identical, the different loading of each stage produces a variation in some of the stage performance characteristics. The voltage gains for each amplifier stage is calculated to be:

$$A_{V1} = \frac{-150\,(2.2//10.47//66.55)}{66.55} = -3.9887, \quad \text{and} \quad A_{V2} = \frac{-150\,(2.2//2.7)}{66.55} = -2.7323.$$

The overall voltage gain is given by the product of the individual stage gains and a voltage division at the input, as originally derived in Equation (6.2):

$$A_V = \frac{v_o}{v_s} = (A_{V2})\,(A_{v1}) \left(\frac{R_i}{R_i + R_s} \right) = (-3.9887)\,(-2.7323) \left(\frac{9.05}{9.05 + 0.1} \right) \approx 10.8.$$

The current gain can be derived from the voltage gain and the various resistances:

$$A_I = \frac{i_{load}}{i_{source}} = \left(\frac{i_{load}}{v_o} \right) \left(\frac{v_o}{v_s} \right) \left(\frac{v_s}{i_{source}} \right) = \left(\frac{1}{R_{load}} \right) (A_V)\,(R_i + R_s) \approx 36.5.$$

All required amplifier performance characteristics have been calculated: the problem statement in this example does not require that AC and DC performance be added.

While the capacitive coupling of amplifier stages has its primary advantage in the decoupling of the individual stage quiescent conditions, there are disadvantages that must be considered. The addition of capacitors may seriously degrade the low-frequency response of an amplifier. In addition, the decoupling of quiescent conditions necessitates the individual biasing of each transistor into the forward-active (for BJTs) or saturation (for FETs) regions. Individual biasing can significantly increase the numbers of bias elements (in discrete amplifiers these elements are usually resistors) which will increase the size, cost, and power consumption of an amplifier. It is therefore advantageous, whenever possible, to directly couple amplifier stages. Capacitive coupling of the input source and the load is often unavoidable due to the DC offsets often necessary in these simple amplifier stages.

An example of a two-stage cascade-connected amplifier with directly-coupled stages is shown in Figure 6.2. The bias for the second transistor stage (the BJT for this amplifier) is dependent on the quiescent conditions of the first transistor stage. The choice to use dependent biasing

rather than capacitively couple independent stages has eliminated, in this case, two bias resistors and a capacitor from the design.

Under certain circumstances, is might be possible to eliminate other elements from this amplifier. The purpose of R_g is to ensure that the quiescent voltage at the gate of Q1 is at zero potential. If the designer is absolutely sure the input source, v_s, has no DC bias, the resistor R_g and its associated input capacitor could also be eliminated from this design.

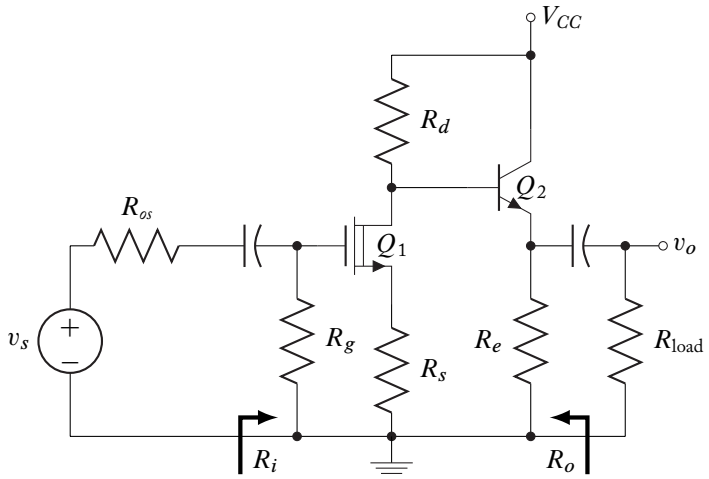


Figure 6.2: A cascade-connected amplifier with direct coupling of stages.

Example 6.2

The two-stage cascade-connected amplifier shown in Figure 6.2 is comprised of two directly-connected simple stages. The transistors have characteristic parameters:

$$\beta_F = 150 \qquad V_A = 350\,\text{V} \qquad \text{(Silicon BJT)},$$

and

$$V_{PO} = -3.5\,\text{V} \qquad I_{DSS} = 10\,\text{mA} \qquad V_A = 250\,\text{V} \qquad \text{(FET)}.$$

The circuit resistors are given as:

$$\begin{aligned} R_g &= 1\,\text{M}\Omega & R_e &= 2.7\,\text{k}\Omega, \\ R_d &= 1.5\,\text{k}\Omega & R_{os} &= 100\,\Omega, \\ R_s &= 130\,\Omega & R_{load} &= 2.2\,\text{k}\Omega\,. \end{aligned}$$

The power supply voltage is: $V_{CC} = 15\,\text{V}$.

Determine the AC voltage and current gain (from the source to the load) and the input and output resistances (as shown) for this amplifier.

Solution

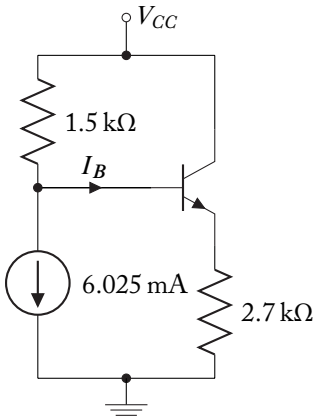
The quiescent conditions for the FET are determined with the usual expressions relating I_D and V_{GS} in the saturation region:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_{PO}}\right)^2 = -\frac{V_{GS}}{R_s}$$
$$= 10\,\text{mA}\left(1 - \frac{V_{GS}}{-3.5}\right)^2 = -\frac{V_{GS}}{130}.$$

Solving this equation yields the FET quiescent conditions:

$$V_{GS} = -0.7833\,\text{V} \qquad I_D = 6.025\,\text{mA}.$$

The BJT quiescent conditions depend on the DC circuit shown at the right. The base and collector currents by making a Thévenin equivalent of the circuit connected to the base of the BJT:



$$R_{th} = 1.5\,\text{k}\Omega \qquad V_{th} = 15 - 6.025(1.5) = 5.962.$$

The BJT base and collector currents are then found to be:

$$I_B = 12.86\,\mu\text{A} \quad \text{and} \quad I_C = 1.93\,\text{mA}.$$

Checking to see if the transistors are in the appropriate regions yields:

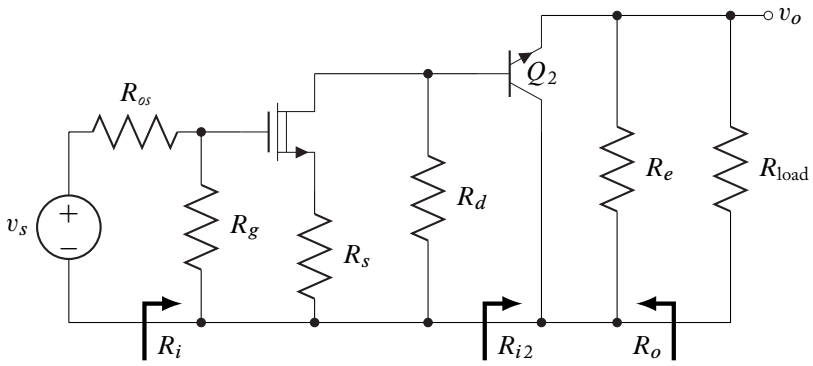
$$V_{CE} = 15 - I_C(2.7\,\text{k}) = 9.79\,\text{V} \geq 0.2$$
$$V_{DS} = 15 - 1.5\,\text{k}(I_D + I_B) - 130 I_D = 5.16\,\text{V} \geq V_{GS} - V_{PO} = 2.72.$$

The transistors are appropriately biased: the transistor AC parameters then are calculated to be:

$$h_{fe} = \beta_F = 150 \quad \text{and} \quad h_{ie} = (\beta_F + 1)\left(\frac{\eta V_t}{|I_C|}\right) = 2.04\,\text{k}\Omega$$

$$g_m = \frac{2I_D}{(V_{GS} - V_{PO})} = 4.435\,\text{mA/V}, \qquad r_d = \left|\frac{V_A}{I_D}\right| = 41.49\,\text{k}\Omega \quad \text{and} \quad \mu = g_m r_d = 184.0.$$

The AC model for the circuit consists of a common-source amplifier stage followed by a common-collector stage. The performance parameters for these simple stages were derived in Chapter 4 (Book 1).



The total input resistance, R_i, is the parallel combination of R_g and the input resistance of the common-source stage:

$$R_i = R_g // \infty = R_g = 1\,\text{M}\Omega.$$

The input resistance of the common-collector stage is given by:

$$R_{i2} = h_{ie} + (h_{fe} + 1)(R_e // R_{load}) = 185.1\,\text{k}\Omega.$$

The gain of the common-source stage is:

$$A_{V1} = \frac{-\mu\,(R_d // R_{i2})}{r_d + (R_d // R_{i2}) + (\mu + 1)\,R_s} = -4.085.$$

The gain of the common-collector stage is:

$$A_{V2} = 1 - \frac{h_{ie}}{R_{i2}} = 0.9890.$$

The overall gain is given by:

$$A_V = A_{V1} A_{V2} \left(\frac{R_i}{R_i + R_{os}}\right) = -4.04.$$

The current gain can be derived from the voltage gain and the various resistances:

$$A_I = \frac{i_{load}}{i_{source}} = \left(\frac{i_{load}}{v_o}\right)\left(\frac{v_o}{v_s}\right)\left(\frac{v_s}{i_{source}}\right) = \left(\frac{1}{R_{load}}\right)(A_V)(R_i + R_s) = -1840.$$

The output resistance calculation is the most difficult to perform. The output resistance of the common-collector stage depends on the output resistance of the common-source stage:

$$R_{o2} = \frac{(R_{o1}//R_d) + h_{ie}}{h_{fe} + 1}.$$

The output resistance of the common-source stage is:

$$R_{o1} = r_d + (\mu + 1)R_s = 65.55\,\text{k}\Omega.$$

Therefore,

$$R_{o2} = 23.2\,\Omega$$

and the total output resistance is given by:

$$R_o = R_{o2}//R_e = 23.0\,\Omega.$$

6.1.1 DESIGN CHOICES FOR TRANSISTOR CONFIGURATION IN A CASCADE-CONNECTED AMPLIFIER

The previous example derivations and calculate on of voltage and current gain and input and output resistance apply to any configuration of cascade-connected amplifier. As each stage is added, the gain expression is increased by only one additional term. The individual stages may be any of the three BJT or three FET configurations and any number of these stages may be connected in any order. There are, however, design choices that are better engineering practice than other choices.

The basic reason for choosing a multiple-stage amplifier over a single-stage amplifier are one or more of the following performance characteristics:

- increased amplification
- input impedance modification
- output impedance modification

Common-emitter and common-source amplifier stages are ideal for increased amplification purposes. Each type exhibits significant voltage gain *and* significant current gain. In addition, when

cascade-connected, the relatively high input resistance of these stage configurations does not significantly load previous amplification stages (voltage gain is a function of the load). Common-base and common-gate amplifiers exhibit good voltage gain but no current gain. The relatively low input resistance of these stages also produces a gain-reducing load to previous stages. Consequently, these stages are most useful as low input resistance first stages. Common-collector and common-drain amplifiers have good current gain but no voltage gain. Their relatively high input resistance allows them to follow a amplification stage without seriously decreasing the voltage gain. These two configurations are most useful for low output resistance final stages. In summary, the design choices for a cascade-connected amplifier are usually are based on the following principles:

- First stage should *not* be common-collector or common-drain
  (a) Low input resistance cases: common-base or common-gate
  (b) Other cases: common-emitter or common-source
- Intermediate stages should be common-emitter or common-source
- Final stage should *not* be common-base or common-gate
  (a) Low output resistance cases: common-collector or common-drain
  (b) Other cases: common-emitter or common-source

  Special purpose amplifiers may violate these design principles as seen in Section 6.2.

6.2 DARLINGTON AND OTHER SIMILAR CONFIGURATIONS

In addition to cascade-connected single-transistor amplifiers, there exist several two-transistor configurations that are commonly analyzed and often packaged as signal stages. These particular combinations are unusual in that they seem to violate to configuration principles of good amplifier design as itemized in the last section. The configurations do, however, produce amplifiers with specific, significantly-enhanced properties.

Most common among these configurations are the two Darlington BJT configurations and the Cascode configuration. Mixed BJT and FET combinations are currently not as common as the single-type configurations. The BiFET (BiCMOS) Darlington seems most promising of these newer technology combinations.

6.2.1 THE DARLINGTON CONFIGURATIONS

The Darlington two-transistor amplifier configurations consist of a pair of BJTs connected so that the emitter of the input transistor couples directly, in an AC sense, into the base of the output transistor. A DC biasing current source is also commonly present at this transistor interconnection node. The output is taken at either the collector or the emitter of the second transistor. Thus,

in a Darlington connected BJT pair, the first transistor stage is a common-collector while the second stage can be either common-collector or common-emitter. Figure 6.3 shows the two basic Darlington configurations.[3]

The Darlington Configurations incorporate an additional transistor so that overall circuit performance is altered significantly:

- Current Gain is Increased, and
- Input Resistance is Increased.

These increases in current gain and input resistance are by a factor of approximately β_F. The exact change in circuit performance requires careful analysis.

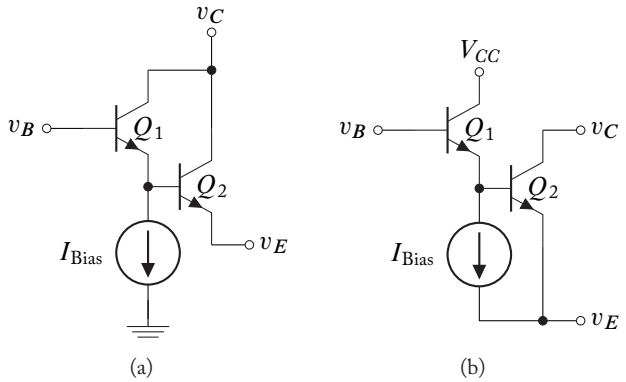


Figure 6.3: Darlington configurations: (a) Dual common-collector pair; (b) Common-collector—common-emitter pair.

It is common practice to analyze these two-transistor pairs as a single subcircuit. This subcircuit takes on many of the characteristic properties of a single BJT, modified due to the presence of two transistors. The subcircuit nodes that correspond to the so called "composite transistor" are labeled in Figure 6.4 as B^C, C^C and E^C.

The fourth terminal in Darlington subcircuits exists solely for DC biasing. Commercially packaged Darlingtons allow for the fourth terminal in several different ways:

- by providing a separate external connection (a four terminal package),
- internally providing for the bias current or voltage source with additional circuitry within the package (a three terminal package), or,
- in the case of the bias current source, occasionally eliminating it entirely (a three terminal package). This case is equivalent to setting the bias current source, I_{Bias}, to zero value.

[3]Other slight variations occur. These variations are due a variety of possible connections for the voltage and current biasing sources, V_{CC} and I_{Bias}.

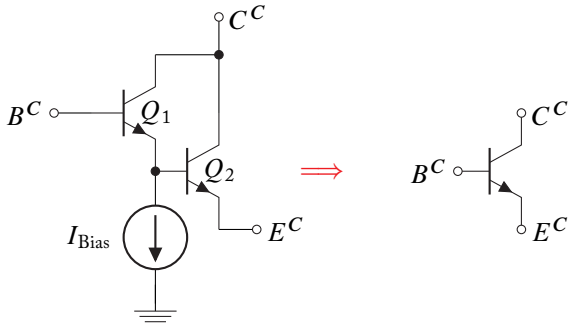


Figure 6.4: Modeling a dual common-collector darlington pair as a composite transistor.

6.2.2 THE DUAL COMMON-COLLECTOR DARLINGTON CONFIGURATION

The Dual Common-Collector Darlington Configuration (Figure 6.4) is the most common of the two Darlington Configurations: a wide variety of commercial packages of this configuration of transistors is available. In this configuration, the base of the composite transistor is the base of the first BJT (Q1), the two BJT collectors are connected together to form the composite collector, and the emitter of the second BJT (Q2) forms the composite emitter. As one might expect, the composite transistor can operate in all four regions that are usually associated with BJTs: the cut-off, saturation, forward-active, and inverse-active regions. Simplified models, and their equivalent circuits, of composite transistor operation in each region are of the same form as those developed for BJTs in Section 3.4 (Book 1). However, the composite transistor will have characteristic parameters in each of these regions that vary from typical BJT values.

In the *cut-off region,* the composite transistor operates as three terminals with open circuits between. In order to turn the subcircuit on, both BJT base-emitter junctions must become forward biased. Since the composite base-emitter consists of two BJT base-emitter junctions, the typical turn-on base-emitter voltage for this composite transistor[4] is approximately double that of a single BJT:

$$V_{BE(on)} \approx 1.2\,\text{V}. \tag{6.3}$$

The *saturation region* is modeled by two voltage sources: one modeling the base-emitter terminal pair and the other modeling the collector-emitter terminal pair. The composite base-emitter is modeled by two ON BJTs. Thus, in the saturation region,

$$V_{BE(sat)} \approx 1.6\,\text{V}. \tag{6.4}$$

[4]For simplicity of discussion, all values given in this section will be typical for configurations using Silicon *npn* transistors. Darlington pairs constructed with *pnp* transistors will have similar values with appropriate sign differences. These sign differences are discussed in Chapter 3 (Book 1).

The transition from the saturation region into the forward-active region occurs when the collector-emitter voltage of Q1 becomes too large. At this collector-emitter voltage, Q2 is in the forward-active region ($V_{CE} > 0.2\,\text{V}$). Thus, the composite collector-emitter voltage is the sum of the saturation collector-emitter voltage of Q1 and the forward-active base-emitter voltage of Q2:

$$V_{CE(sat)} \approx 0.9\,\text{V}. \tag{6.5}$$

The *forward-active region* is modeled by the ratio of collector current to base current and the base-emitter voltage. The current ratio can be derived by observing that the composite collector current is the sum of the individual collector currents:

$$\begin{aligned} I_C &= I_{C1} + I_{C2} && (6.6)\\ &= \beta_{F1} I_{B1} + \beta_{F2} I_{B2} \\ &= \beta_{F1} I_{B1} + \beta_{F2} \left[(\beta_{F1} + 1) I_{B1} - I_{Bias}\right]. && (6.7) \end{aligned}$$

For large values of β_F, this expression is commonly approximated as:

$$I_C \approx \beta_{F1}\beta_{F2} I_{B1} - \beta_{F2} I_{Bias}. \tag{6.8}$$

Incremental changes in the composite collector current are proportional to the *product* of the BJT current gains: consequently it can be very large. The composite base-emitter voltage is the sum of the forward active base-emitter voltages for the two BJTs:

$$V_\gamma \approx 1.4\,\text{V}. \tag{6.9}$$

The emitter current is calculated to be:

$$-I_E = (\beta_{F1} + 1)(\beta_{F2} + 1) I_B - (\beta_{F2} + 1) I_{Bias}. \tag{6.10}$$

Due to the addition, in the composite transistor, of a fourth terminal with non-zero current, the current flowing out the emitter terminal is, in general, not equal to the sum of the base and emitter currents.

The *inverse-active region* is similar to the forward-active region. Darlington circuits rarely enter into this region since the multiple transistor design brings no benefits over single transistors operating in this region.

Small-Signal h-Parameters

When a Darlington pair in the forward-active region is used in an amplifier, it is appropriate to model the composite transistor with an h-parameter model. The composite h-parameters can be obtained from the h-parameter models of the individual BJTs as is shown in Figure 6.5.

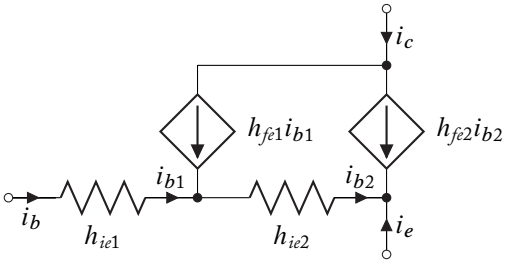


Figure 6.5: The AC model for a dual common-collector Darlington pair.

The collector current is the sum of the individual collector currents

$$\begin{aligned} i_c &= i_{c1} + i_{c2} \qquad (6.11)\\ &= h_{fe1}i_{b1} + h_{fe2}i_{b2} \\ &= h_{fe1}i_{b1} + h_{fe2}(h_{fe1}+1)i_{b1} \\ &= (h_{fe2}+1)(h_{fe1}+1)i_{b1} - i_{b1} \qquad (6.12)\end{aligned}$$

For large values of the individual BJT current gain, this expression is commonly approximated as:

$$i_c \approx h_{fe1}h_{fe2}i_{b1}$$

or

$$h_{fe} \approx h_{fe1}h_{fe2} = \beta_{F1}\beta_{F2}. \qquad (6.13)$$

The composite current gain is the product of the current gains: in general, this is a very large quantity. The input resistance of the composite circuit is given as:

$$h_{ie} = h_{ie1} + (h_{fe1}+1)h_{ie2}. \qquad (6.14)$$

The input resistance has been multiplied significantly and is also a very large quantity. It should be noted that the composite transistor input resistance parameter, h_{ie}, can not be obtained from the composite collector current in the same manner as with a BJT: the value obtained by that process will be much too small. However, similar operations can be performed. The exact value of h_{ie} depends on the collector current I_C as well an on I_{Bias}, but a good approximation can be made that is independent of I_{Bias}. Two common bias schemes are:

- $I_{Bias} = 0$
- I_{Bias} set so that the two BJT collector currents are identical.

In the first case, the two collector currents are approximately[5] different by a factor of β_{F2}:

$$I_{C1} \approx \frac{I_C}{\beta_{F2}+1} \qquad \text{and} \qquad I_{C2} \approx \frac{\beta_{F2} I_C}{\beta_{F2}+1}. \tag{6.15}$$

The individual BJT parameters can be calculated from these collector currents using Equation (5.21):

$$h_{ie1} = \left(h_{fe1}+1\right)\frac{\eta V_t}{|I_{C1}|} = \left(\beta_{F1}+1\right)\left(\beta_{F2}+1\right)\frac{\eta V_t}{|I_C|} \tag{6.16}$$

$$h_{ie2} = \left(h_{fe2}+1\right)\frac{\eta V_t}{|I_{C2}|} = \frac{\left(\beta_{F2}+1\right)^2}{\beta_{F2}}\frac{\eta V_t}{|I_C|}. \tag{6.17}$$

These two values are combined with Equation (6.13) to find h_{ie}:

$$h_{ie} = \left[\left(\beta_{F1}+1\right)\left(\beta_{F2}+1\right) + \frac{\left(h_{fe1}+1\right)\left(\beta_{F2}+1\right)^2}{\beta_{F2}}\right]\frac{\eta V_t}{|I_C|}, \tag{6.18}$$

which, for large current gains, can be approximated as:

$$h_{ie} \approx 2\left(\beta_{F1}+1\right)\left(\beta_{F2}+1\right)\frac{\eta V_t}{|I_C|} \approx 2\beta_{F1}\beta_{F2}\frac{\eta V_t}{|I_C|}. \tag{6.19}$$

In the second case, $I_{C1} = I_{C2} = 0.5 I_C$. This equality of current leads to:

$$h_{ie} = \left(\beta_{F1}+1\right)\frac{2\eta V_t}{|I_{C1}|} + \left(\beta_{F1}+1\right)\left(\beta_{F2}+1\right)\frac{2\eta V_t}{|I_C|} \tag{6.20}$$

which, for large current gains, can be approximated as:

$$h_{ie} = 2\left(\beta_{F1}+1\right)\left(\beta_{F2}+2\right)\frac{\eta V_t}{|I_C|} \approx 2\beta_{F1}\beta_{F2}\frac{\eta V_t}{|I_C|}. \tag{6.21}$$

Notice that the approximate expressions contained in Equations (6.19) and 6.21 are identical: they are a good approximation for h_{ie} in either bias scheme.

Consideration of the output admittance parameter, h_{oe}, does not significantly alter the expressions for h_{fe} or h_{ie}. The composite output admittance parameter is dependent on the output admittance of both transistors:

$$h_{oe} \approx h_{oe2} + (1 + h_{fe2})h_{oe1}. \tag{6.22}$$

One must remember that each output admittance parameter depends on the collector current in each transistor, not the total collector current. If the Bias current, I_{Bias}, is zero,

$$h_{oe} \approx 2\left|\frac{I_C}{V_{A2}}\right|. \tag{6.23}$$

[5]There is an additional term of $(1 + 1/h_{fe1})$ in the ratio. For reasonably large current gains this term is approximately unity. This slight variation has been ignored to simplify the derivation without significantly changing the results.

If the I_{Bias} is set so that the two transistor currents are equal, the output admittance is greatly increased:

$$h_{oe} = (h_{fe2} + 2)\left|\frac{I_C}{V_A}\right|. \tag{6.24}$$

Each of these two expressions has the effect of reducing the output resistance of the composite transistor as compared to a single transistor. The reduction factor lies between 2 and $h_{fe2} + 2$ depending on the value of I_{Bias}.

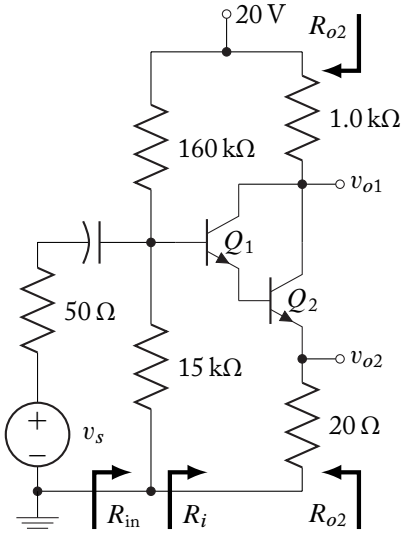
Example 6.3
The given circuit is constructed with Silicon BJTs with parameters:

$$\beta_F = 100$$
$$V_A = 400\,\text{V}.$$

Determine the two voltage gains:

$$A_{V1} = \frac{v_{o1}}{v_s} \quad \text{and} \quad A_{V2} = \frac{v_{o2}}{v_s},$$

the current gains (defined as the ratio of current in the output resistors to the current in the source), and the indicated AC resistances.



Solution:

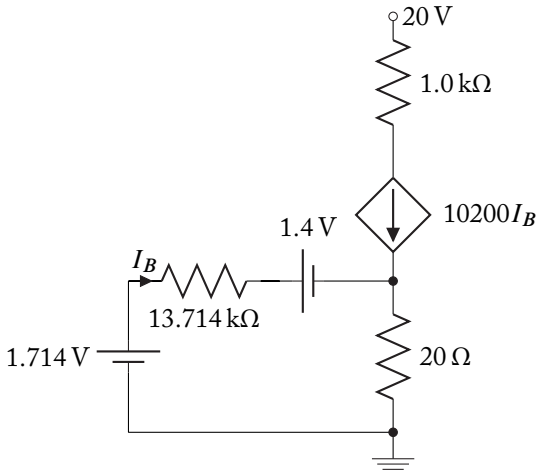
The given circuit employs a dual common-collector Darlington pair with the bias current source set to zero value. The procedure for finding the required AC circuit parameters follows the same guidelines as those presented in Chapter 5.

The quiescent conditions for the composite transistor are obtained by inserting a DC model of the transistor into the circuit. The two significant composite transistor parameters are given by Equations (6.7) and (6.9):

$$V_\gamma = 1.4\,\text{V} \quad \text{and} \quad \beta_F = 10200.$$

After the base circuit is replaced by its Thévenin equivalent, the resultant circuit must be analyzed to find the quiescent conditions:

$$\begin{aligned} I_B &= \frac{1.714 - 1.4}{13.714\,\text{k} + 10201\,(20)} = 1.443\ \mu\text{A} \\ I_C &= 10200 I_B = 14.723\,\text{mA} \\ I_E &= (101)^2 I_B = -14.724\,\text{mA}. \end{aligned}$$



The collector-emitter voltage must be checked to make sure the composite transistor is in the forward active region:

$$V_{CE} = 20 - 1\,\text{k}(I_C) - 20(-I_E) = 4.98\,\text{V} > 0.9\,\text{V}.$$

The composite transistor is in the forward-active region. The AC parameters can now be determined:

$$h_{ie} \approx 2\beta_{F1}\beta_{F2}\frac{\eta V_t}{|I_C|} = 35.32\,\text{k}\Omega \quad \text{and} \quad h_{fe} \approx \beta_{F1}\beta_{F2} = 10\,\text{k}.$$

The amplifier circuit is, depending on which output is taken, of the form of a common-emitter (with an emitter resistor) or a common-collector amplifier. The amplifier performance summary of Section 5.6 is used to determine the performance of this amplifier. The input resistance at the base of the composite transistor is given by:

$$R_i = h_{ie} + h_{fe}(20) = 235\,\text{k}\Omega\,.$$

The input resistance to the total amplifier is:

$$R_{in} = R_i // 15\,\text{k}\Omega // 160\,\text{k}\Omega = 12.96\,\text{k}\Omega.$$

A_{V1} is the composite common-emitter gain:

$$A_{V1} = \left(\frac{12.96\,\text{k}\,\Omega}{12.96\,\text{k}\,\Omega + 50\,\Omega}\right)\left(-\frac{10\,\text{k}\,(1\,\text{k}\,\Omega)}{235\,\text{k}\,\Omega}\right) = -42.5.$$

The corresponding current gain is easily derived from previously obtained quantities:

$$\begin{aligned} A_{I1} = \frac{i_{o1}}{i_s} &= \left(\frac{i_{o1}}{v_o}\right)\left(\frac{v_o}{v_s}\right)\left(\frac{v_s}{i_s}\right) = \left(\frac{1}{R_{load}}\right)(A_{V1})\,(R_{in}) \\ &= \left(\frac{1}{1\,\text{k}\Omega}\right)(-42.5)\,(12.96\,\text{k}\Omega) = -551 \end{aligned}$$

A_{V2} is the composite common-collector gain:

$$A_{V2} = \left(\frac{12.96\,\text{k}\,\Omega}{12.96\,\text{k}\,\Omega + 50\,\Omega}\right)\left(1 - \frac{35.32\,\text{k}\,\Omega}{235\,\text{k}\,\Omega}\right) = 0.850.$$

The corresponding current gain is given by:

$$\begin{aligned} A_{I2} = \frac{i_{o2}}{i_s} &= \left(\frac{i_{o2}}{v_o}\right)\left(\frac{v_o}{v_s}\right)\left(\frac{v_s}{i_s}\right) = \left(\frac{1}{R_{load}}\right)(A_{V2})\,(R_{in}) \\ &= \left(\frac{1}{20\,\Omega}\right)(0.850)\,(12.96\,\text{k}\Omega) = 551. \end{aligned}$$

As expected, the two current gains are very nearly the same in magnitude.

The output resistance of the common-emitter (with an emitter resistor) amplifier is approximately the load resistor:

$$R_{o1} \approx 1.0\,\text{k}\Omega.$$

If h_{oe} is considered to be non-zero, the output resistance can be calculated using Equations (6.23) and (5.75):

$$\begin{aligned} h_{oe} &\approx 2\left|\frac{I_C}{V_{A2}}\right| = 2\frac{14.723\ \text{mA}}{400\ \text{V}} = 73.6\ \mu\text{S} \quad \Rightarrow \quad r_o = 13.6\ \text{k}\Omega \\ R_o &= \frac{v}{i} = \{R_e // (R_s + h_{ie})\} + r_o\left\{1 + \frac{h_{fe}R_e}{R_e + h_{ie} + R_s}\right\} = 90.4\ \text{k}\Omega \\ R_{o1} &= 1.0\,\text{k}\Omega // 90.4\,\text{k}\Omega = 990\,\Omega \approx 1.0\,\text{k}\Omega. \end{aligned}$$

The common-collector output resistance is given by:

$$R_{o2} = \frac{(50\,\Omega // 13.714\,\text{k}\,\Omega) + 35.32\,\text{k}\,\Omega}{10\,\text{k} + 1} = 3.54\,\Omega.$$

6.2.3 THE COMMON-COLLECTOR—COMMON-EMITTER DARLINGTON PAIR

The Common-Collector—Common-Emitter (CC-CE) Darlington Pair is not as common as the Dual Common-Collector Pair. The electrical properties of the two types are very similar, except the CC-CE Pair always requires at least four terminal connections. If the CC-CE pair is to be commercially packaged, it either requires the inclusion of an internal DC current source, I_{Bias}, or necessitates that the source be zero-valued (replaced by an open).

The analysis procedure of this configuration is similar to that of the Dual Common-Collector Darlington. Figure 6.6 identifies the correspondence between the circuit terminals and those of the "composite transistor" equivalent.

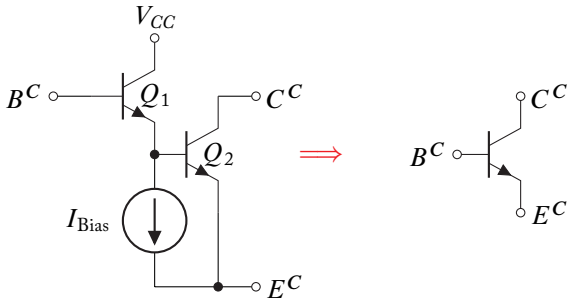


Figure 6.6: Modeling a CC-CE Darlington pair as a composite transistor.

In the *cut-off region,* the composite transistor operates as three terminals with open circuits between. In order to turn the subcircuit on, both BJT base-emitter junctions must become forward biased. Since the composite base-emitter consists of two BJT base-emitter junctions, the typical turn-on base-emitter voltage for this composite transistor is approximately double that of a single BJT:

$$V_{BE(on)} \approx 1.2\,\text{V}.$$

The *saturation region* is modeled by two voltage sources: one modeling the base-emitter terminal pair and the other modeling the collector-emitter terminal pair. The composite base-emitter is modeled by two ON BJTs. Thus, in the saturation region,

$$V_{BE(sat)} \approx 1.6\,\text{V}. \tag{6.25}$$

The composite collector-emitter voltage is the saturation collector-emitter voltage of Q2:

$$V_{CE(sat)} \approx 0.2\,\text{V}. \tag{6.26}$$

The *forward-active region* is modeled by the ratio of collector current to base current and the base-emitter voltage. The current ratio can be derived by observing that the composite collector current

is the same as the collector current of Q2:

$$\begin{aligned} I_C &= I_{C2} && (6.27)\\ &= \beta_{F2} I_{B2} \\ &= \beta_{F2}[(\beta_{F1}+1)I_{B1} - I_{Bias}]. && (6.28)\end{aligned}$$

For large values of β_F, this expression is the same as the dual common-collector Darlington:

$$I_C \approx \beta_{F1}\beta_{F2} I_{B1} - \beta_{F2} I_{Bias}. \tag{6.29}$$

Incremental changes in the composite collector current are proportional to the *product* of the BJT current gains: consequently it can be very large. The composite base-emitter voltage is the sum of the forward active base-emitter voltages for the two BJTs:

$$V_\gamma \approx 1.4\,\text{V}. \tag{6.30}$$

The emitter current is calculated to be:

$$\begin{aligned} -I_E &= (\beta_{F2}+1)I_{B2} + I_{Bias} \\ -I_E &= (\beta_{F1}+1)(\beta_{F2}+1)I_B - (\beta_{F2})I_{Bias}. && (6.31)\end{aligned}$$

Due to the addition, in the composite transistor, of a fourth terminal with non-zero current, the current flowing out the emitter terminal is, in general, not equal to the sum of the base and emitter currents.

The *inverse-active region* is similar to the forward-active region. Darlington circuits rarely enter into this region since the multiple transistor design brings no benefits over single transistors operating in this region.

Small-signal h-Parameters

When a Darlington pair in the forward-active region, the composite h-parameters can be obtained from the h-parameter models of the individual BJTs as is shown in Figure 6.7.

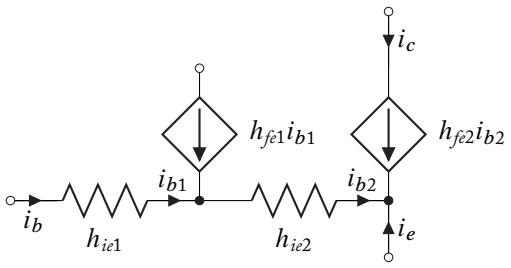


Figure 6.7: The AC model for a common-collector—common emitter Darlington pair.

The collector current is collector current of the Q2:

$$\begin{aligned} i_c &= i_{c2} && (6.32)\\ &= h_{fe2} i_{b2} \\ &= h_{fe2}(h_{fe1}+1) i_{b1}. && (6.33) \end{aligned}$$

For large values of the individual BJT current gain, this expression is approximated as:

$$i_c \approx h_{fe1}\, h_{fe2}\, i_{b1} \quad \text{or} \quad h_{fe} \approx h_{fe1}\, h_{fe2}. \tag{6.34}$$

The composite current gain is the product of the current gains: in general, this is a very large quantity. The input resistance of the composite circuit is given as:

$$h_{ie} = h_{ie1} + (h_{fe1}+1) h_{ie2}. \tag{6.35}$$

The input resistance has been multiplied significantly and is also a very large quantity. It should be noted that the composite transistor input resistance parameter, h_{ie}, can not be obtained from the composite collector current in the same manner as with a BJT: the value obtained by that process will be much too small. However, similar operations can be performed. The exact value of h_{ie} depends on the collector current I_C as well an on I_{Bias}, but a good approximation can be made that is independent of I_{Bias}. Two common bias schemes are:

- $I_{Bias} = 0$
- I_{Bias} set so that the two BJT collector currents are identical.

In the first case, the two collector currents differ[6] by a factor of β_{F2}:

$$I_{C1} \approx \frac{I_C}{\beta_{F2}} \quad \text{and} \quad I_{C2} = I_C. \tag{6.36}$$

The individual BJT parameters can be calculated from these collector currents using Equation (5.21):

$$h_{ie1} = \left(h_{fe1}+1\right) \frac{\eta V_t}{|I_{C1}|} = (\beta_{F1}+1)\,(\beta_{F2})\, \frac{\eta V_t}{|I_C|} \tag{6.37}$$

$$h_{ie2} = \left(h_{fe2}+1\right) \frac{\eta V_t}{|I_{C2}|} = (\beta_{F2}+1)\, \frac{\eta V_t}{|I_C|}. \tag{6.38}$$

These two values are combined with Equation (6.35) to find h_{ie}:

$$h_{ie} = \left[(\beta_{F1}+1)\,(\beta_{F2}) + \left(h_{fe1}+1\right)(\beta_{F2}+1)\right] \frac{\eta V_t}{|I_C|}, \tag{6.39}$$

[6] As with the Dual Common-Collector Darlington, there is an additional term of $(1 + 1/h_{fe1})$ in the ratio. For reasonably large current gains this term is approximately unity. This slight variation has been ignored to simplify the derivation without significantly changing the results.

which, for large current gains, can be approximated as:

$$h_{ie} \approx 2\beta_{F1}\beta_{F2}\frac{\eta V_t}{|I_C|}. \tag{6.40}$$

In the second case, $I_{C1} = I_{C2} = I_C$. This equality of current leads to:

$$h_{ie} = (\beta_{F1}+1)\frac{\eta V_t}{|I_{C1}|} + (\beta_{F1}+1)(\beta_{F2}+1)\frac{\eta V_t}{|I_C|} \tag{6.41}$$

which, for large current gains, can be approximated as:

$$h_{ie} = (\beta_{F1}+1)(\beta_{F2}+2)\frac{\eta V_t}{|I_C|} \approx \beta_{F1}\beta_{F2}\frac{\eta V_t}{|I_C|}. \tag{6.42}$$

Notice that the approximate expressions contained in Equations (6.41) and (6.42) differ by a factor of two: they present a good approximation for the range of h_{ie}.

Consideration of the output admittance parameter, h_{oe}, does not significantly alter the expressions for h_{fe} or h_{ie}. The composite output admittance parameter is that of Q2:

$$h_{oe} = h_{oe2} = \left|\frac{I_C}{V_{A2}}\right|. \tag{6.43}$$

6.2.4 THE CASCODE CONFIGURATION

The cascode configuration consists of a pair of BJTs connected in a Common-Emitter—Common-Base configuration as shown in Figure 6.8. The principal attribute of the cascode configuration of interest here is extremely high output impedance. Other attributes that will be investigated in later chapters include: very good (compared to common-emitter) high-frequency performance and very little reverse transmission. The property of small reverse transmission (signals applied to the output appearing at the input) aids in the design of high-frequency tuned amplifiers.

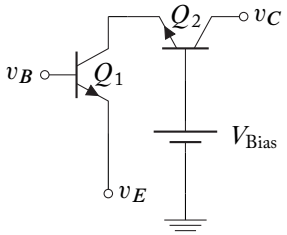


Figure 6.8: The cascode configuration.

The large-signal operating conditions are characterized by the following regional parameters:

$$\begin{aligned} V_{BE(on)} &= 0.6 \qquad V_\gamma = 0.7 \\ V_{BE(SAT)} &= 0.8 \qquad V_{CE(SAT)} = 0.4 \end{aligned} \tag{6.44}$$

with the additional qualifiers that

$$V_C \geq V_{Bias} - 0.6 \qquad V_E \leq V_{Bias} - 1.0. \tag{6.45}$$

Small-Signal h-Parameters

When the BJTs of a Cascode are in the forward-active region, two of the composite h-parameters can be obtained directly from Table 5.7:

$$h_{ie} = h_{ie1} \approx (\beta_{F1}+1)\,\frac{\eta V_t}{|I_C|} \tag{6.46}$$

and

$$h_{fe} = h_{fe1}\left(\frac{h_{fe2}}{h_{fe2}+1}\right) \approx h_{fe1}. \tag{6.47}$$

The output admittance parameter, h_{oe}, is calculated by calculating the output admittance of the small-signal equivalent circuit with the base current set to zero (Figure 6.9).

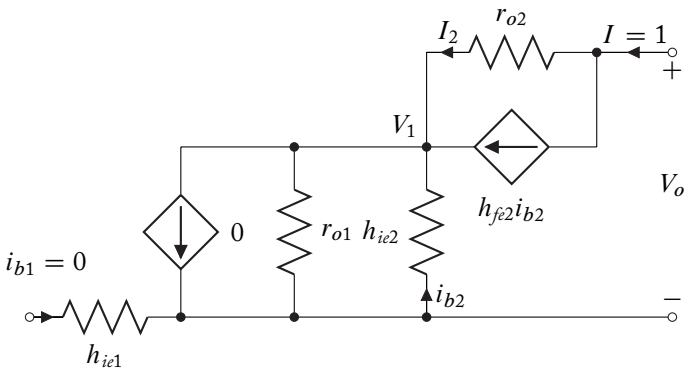


Figure 6.9: Equivalent circuit for calculation of cascode h_{oe}.

The test for h_{oe} requires that there be zero base current: this condition implies that the output impedance of the common-emitter BJT is in parallel with the input impedance of the common-base BJT. Application of a unity current to the output terminals yields:

$$i_{b2} = \frac{-r_{o1}}{r_{o1}+h_{ie2}} \quad \text{and} \quad V_1 = \frac{r_{o1}h_{ie2}}{r_{o1}+h_{ie2}}.$$

The resultant voltage at the output terminals is determined by finding the current through h_{oe2} and using Kirchhoff's Voltage Law:

$$I_2 = 1 - h_{fe2} i_{b2} = 1 + h_{fe2} \frac{r_{o1}}{r_{o1} + h_{ie2}}$$

then,

$$V = V_1 + I_2 r_{o2}$$

or

$$V = \frac{r_{o1} h_{ie2}}{r_{o1} + h_{ie2}} + \left(1 + h_{fe2} \frac{r_{o1}}{r_{o1} + h_{ie2}}\right) r_{o2}.$$

The output admittance is the ratio of the current I to the voltage V:

$$h_{oe} = \frac{1}{\dfrac{r_{o1} h_{ie2}}{r_{o1} + h_{ie2}} + \left(1 + h_{fe2} \dfrac{r_{o1}}{r_{o1} + h_{ie2}}\right) r_{o2}} \approx \frac{h_{oe2}}{1 + h_{fe2}}. \tag{6.48}$$

The output admittance is an extremely small quantity. It can be calculated from the quiescent conditions to be:

$$h_{oe} \approx \frac{1}{h_{fe2}} \left| \frac{I_C}{V_{A2}} \right|. \tag{6.49}$$

In that the output impedance is the reciprocal of output admittance, the output impedance of a cascode configuration has been shown to be larger than that of a single common-emitter stage by a factor of $1 + h_{fe}$.

A FET variation of the cascode configuration is often found in analog design. The FET cascode consists of a Common-Source—Common Gate connection. As one might expect, the only major change over a single common-source stage is increased output impedance. Since the amplification of a common-source stage is highly dependent on the output impedance, r_d, of the FET, the FET cascode will have greatly improved voltage gain. One drawback is that maximum symmetrical swing may be degraded with the FET cascode.

6.2.5 THE BIFET DARLINGTON CONFIGURATION

No useful all-FET Darlington circuits exist: the potential for increased input impedance and current gain have little significance in FET circuitry. There is, however, a useful Darlington circuit connection that combines the properties of FETs and BJTs. In this configuration the input BJT of a Darlington pair is replaced by a FET (Figure 6.10). The connection retains the near-infinite input impedance of the FET and, with the addition of the BJT, attains a larger effective composite transconductance, g_m and a lower output resistance, r_d. Common technologies currently in use

that allow BJTs and FETs to be produced on the same substrate include the BiCMOS and BiFET technologies.[7]

Previous analysis of similar circuitry suggests that the formation of a composite FET is appropriate. Quiescent analysis of the BiCMOS Darlington leads to the following relationships:

$$I_D^C = K^C \left[V_{GS}^C - V_T^C \right]^2 - \beta_F I_{Bias} \tag{6.50}$$

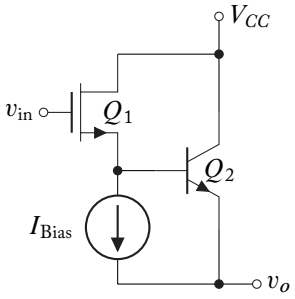


Figure 6.10: BiCMOS Darlington configuration.[8]

where

I_D^C = the composite drain current,
V_{GS}^C = the composite gate-source voltage,
$V_T^C = V_T + V_\gamma$ = the composite threshold voltage, and
$K_C = (1 + \beta_F)K$ = the composite transconductance factor.

Similarly, a small-signal analysis of the composite transistor can be performed in a similar manner as with previous configurations. Each transistor is replaced by its appropriate small-signal model, a voltage source is applied to the composite transistor gate-source terminals and the short-circuit current gain, g_m, is calculated:

$$g_m^C = \frac{\left(1 + h_{fe}\right) g_m}{1 + h_{ie}\left(g_m + 1/r_d\right)}. \tag{6.51}$$

The Thévenin output resistance, r_d, is calculated by setting the composite transistor gate-source voltage to zero and applying a current to the drain-source terminals. The results of such operations leads to:

$$r_d^C = \frac{r_d + (\mu + 1)\, h_{ie}}{h_{fe} + 1}. \tag{6.52}$$

[7]BiCMOS implies CMOS and BJT transistors on the same substrate. Although BiFET is a more general term, it usually implies JFETs and BJTs.

[8]As with the BJT Darlington circuits, the exact connection of the biasing current source may vary in particular applications. The effect is only in the quiescent conditions and the individual small-signal parameters of each transistor: general performance *relationships* are unchanged.

As expected, the addition of a common-collector stage to the FET did not significantly change the voltage gain of the composite transistor ($\mu = g_m r_d$).

6.3 EMITTER-COUPLED AND SOURCE-COUPLED PAIRS

Emitter-coupled and source-coupled pairs of transistors are widely used to form the basic element of differential amplifiers with the most common application being the input stage of an Operational Amplifier. The output of such amplifier stages is proportional to the difference in the input voltages and has a high Common-Mode Rejection Ratio. High CMRR allows the input to be differential or single (one input at a fixed voltage). The output can be similarly differential or single (as in the OpAmp).

Another useful property of emitter-coupled and source-coupled amplifier stages is that they can be cascaded without interstage coupling capacitors: any common-mode DC offset that may be present has a negligible effect on the performance of any stage. Input impedance is typically high for FET pairs and moderate for BJT pairs: output impedance is moderate for all types.

6.3.1 EMITTER-COUPLED PAIRS

The basic topology for an emitter-coupled pair is shown in Figure 6.11. In order to form a good differential amplifier, the circuit must by a symmetric network: the transistors must have similar properties and corresponding collector resistances should have identical values ($R_{c1} = R_{c2} = R_c$). These collector resistances are often discrete resistors; in integrated circuit applications, they are more often active loads.[9] In integrated circuit realizations of an emitter-coupled pair, the biasing network is typically in the form of a transistor current source; in other realizations it can be as simple as a single resistor. For generality, the biasing network is shown in its most general form as a Norton equivalent source.

The topology of this amplifier is very similar to that of the input section of an Emitter-Coupled Logic gate. Previous explorations of that logic gate family[10] found that a linear region of amplification exists in the transition region between the two logic levels. This region extends over a very small range of input voltage differences: the difference between the voltages at the two BJT base terminals can not exceed a few tenths of a volt before one of the transistors enters the cut-off region and the amplifier saturates. Still, as has been seen in the case of the OpAmp, it is not necessary for the input voltage difference to be large in order to create a highly useful device.

[9] Active loads are discussed in Section 6.5.
[10] Emitter-Coupled Logic gates are discussed in Section 3.5 (Book 1).

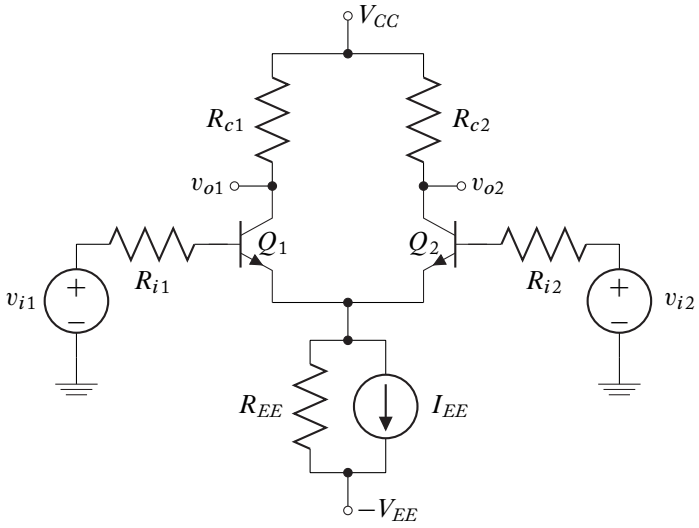


Figure 6.11: A typical emitter-coupled pair circuit diagram.

DC Analysis of the Emitter-Coupled Pair

If the circuit is truly symmetric ($R_{i1} = R_{i2} = R_i$), it can be easily shown that the quiescent BJT collector currents are equal and have value:

$$I_C = \beta_F \left(\frac{V_{EE} + I_{EE} R_{EE} - V_{BE(on)}}{2\,(\beta_F + 1)\,R_{EE} + R_i} \right). \tag{6.53}$$

For values of R_{EE} larger than the output resistance, R_i, of the sources, a good approximation[11] for the collector current is:

$$I_C \approx \frac{\alpha_F}{2} \left(I_{EE} + \frac{V_{EE} - V_{BE(on)}}{R_{EE}} \right).$$

From this derived value of I_C and the BJT characteristic parameters, the usual small-signal BJT h-parameters can be derived:[12]

$$h_{fe} = \beta_F, \qquad h_{ie} = (\beta_F + 1)\,\frac{\eta V_T}{I_C}, \qquad \text{and} \qquad h_{oe} = \frac{I_C}{V_A}.$$

Since the BJT quiescent conditions are identical, each of the two BJTs has these same h-parameters.

[11] This approximation is particularly useful if R_{i1} and R_{i2} are not equal but each smaller than R_{EE}.
[12] The BJT must be in the forward-active region: it is important to check V_{CE} to make sure before continuing.

AC Analysis of the Emitter-Coupled Pair

The most significant performance parameter for a differential amplifier is the differential mode gain. Also of significance is the common-mode rejection ratio: the ratio of differential mode gain to common-mode gain[13] The best path to find these performance parameters is through AC analysis and the use of superposition. The AC equivalent circuit for zero v_{i2} is shown in Figure 6.12.

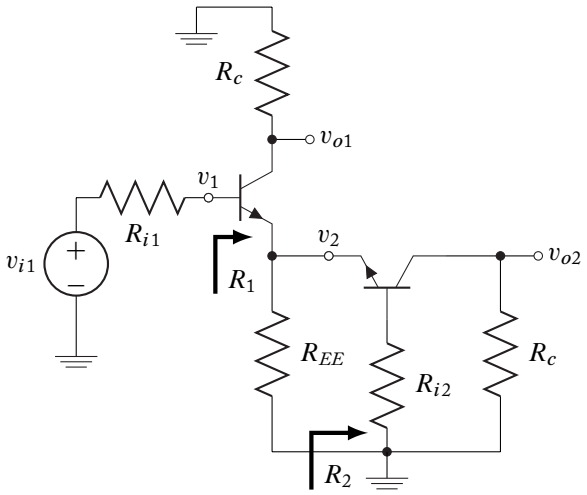


Figure 6.12: AC equivalent circuit for emitter-coupled pair (single input source).

The gain path to v_{o1} is a common-emitter (with an emitter resistor) amplifier stage, while the gain path to v_{o2} is a two-stage cascaded amplifier: a common-collector stage followed by a common-base stage. Table 5.7 provides small-signal amplifier performance parameters to guide the AC analysis of this circuit.[14] Two derived input resistances aid in calculations. The resistance, R_2, is the input resistance of a common-base amplifier:

$$R_2 = \frac{h_{ie} + R_{i2}}{h_{fe} + 1}. \tag{6.54}$$

R_1 is the input resistance of a common-collector amplifier:

$$R_1 = h_{ie} + (h_{fe} + 1)(R_{EE} // R_2). \tag{6.55}$$

Typically, the biasing current source output resistance, R_{EE}, is much greater than the input resistance to the common-base stage, R_2 (a very small value). This relationship leads to a common

[13]For a more complete discussion of common-mode rejection ratio, refer to Section 1.4 (Book 1).
[14]Table 5.7 assumes that the resistors R_c are small compared to $1/h_{oe}$. This may not always be the case. Section 6.4 discussed the effect of large load resistances (in the form of active loads) on amplifier performance.

approximation, $R_{EE}//R_2 \approx R_2$, and

$$R_1 \approx h_{ie} + (h_{fe}+1)\left(\frac{h_{ie}+R_{i2}}{h_{fe}+1}\right) = 2h_{ie} + R_{i2}. \tag{6.56}$$

This approximation for R_1 will be used in early discussions and will be tested for validity in Example 6.5.

The voltage gain to each of the output terminals can now be easily determined. The voltage gain to the v_{o1} terminal is simply the product of a common-emitter amplifier gain and a voltage division:

$$\begin{aligned} A_{V1} &= \frac{v_{o1}}{v_{i1}} = \left(\frac{v_{o1}}{v_1}\right)\left(\frac{v_1}{v_{i1}}\right) \\ A_{V1} &= \left(\frac{-h_{fe}R_c}{R_1}\right)\left(\frac{R_1}{R_1+R_{i1}}\right) \approx \frac{-h_{fe}R_c}{2h_{ie}+R_{i1}+R_{i2}}. \end{aligned} \tag{6.57}$$

The voltage gain to the v_{o2} terminal is the product of a common-base amplifier gain, a common-collector amplifier gain, and a voltage division:

$$\begin{aligned} A_{V2} &= \frac{v_{o2}}{v_{i1}} = \left(\frac{v_{o2}}{v_2}\right)\left(\frac{v_2}{v_1}\right)\left(\frac{v_1}{v_{i1}}\right) \\ A_{V2} &= \left(\frac{h_{fe}R_c}{h_{ie}+R_{i2}}\right)\left(\frac{R_1-h_{ie}}{R_1}\right)\left(\frac{R_1}{R_1+R_{i1}}\right) \end{aligned}$$

rearranging terms gives the expression

$$A_{V2} = \left(\frac{h_{fe}R_c}{R_1+R_{i1}}\right)\left(\frac{R_1-h_{ie}}{h_{ie}+R_{i2}}\right) = -A_{V1}\left(\frac{R_1-h_{ie}}{h_{ie}+R_{i2}}\right). \tag{6.58}$$

Cancellation and substitution of the approximate expression for R_1 leads to a final gain expression:

$$A_{V2} \approx -A_{V1}\left(\frac{2h_{ie}+R_{i2}-h_{ie}}{h_{ie}+R_{i2}}\right) = -A_{V1}. \tag{6.59}$$

The two gain expressions given in equations (6.57) and (6.59) are equal in magnitude:

$$A_{V2} = -A_{V1} = A \tag{6.60}$$

where

$$A \approx \frac{h_{fe}R_c}{2h_{ie}+R_{i1}+R_{i2}}. \tag{6.61}$$

Application of symmetry to this circuit leads to similar expressions for the voltage gains to each output from input v_{i2} when v_{i1} is set to zero value.

$$\frac{v_{o1}}{v_{i2}} = A \quad \text{and} \quad \frac{v_{o2}}{v_{i2}} = -A. \tag{6.62}$$

The total voltage transfer relationships can then be expressed as a superposition of the results of the derivations:

$$\begin{aligned} v_{o1} &= -Av_{i1} + Av_{i2} \\ v_{o2} &= Av_{i1} - Av_{i2}. \end{aligned} \tag{6.63}$$

The differential output, v_{od}, depends only on the differential input:[15]

$$v_{od} = v_o - v_{o2} = (-Av_{i1} + Av_{i2}) - (Av_{i1} - Av_{i2}) = -2A(v_{i1} - v_{i2}) \tag{6.64}$$

$$v_{od} = \frac{-h_{fe}R_c\{v_{i1} - v_{i2}\}}{h_{ie} + 1/2\{R_{i1} + R_{i2}\}}. \tag{6.65}$$

The common output, v_{oc}, is approximately zero:

$$v_{oc} = 1/2(v_{o1} + v_{o2}) = 1/2\{(-Av_{i1} + Av_{i2}) + (Av_{i1} - Av_{i2})\} \approx 0. \tag{6.66}$$

The output resistance of each gain path extremely large looking into the BJT collectors. The output resistance for the total amplifier is approximately equal to R_c.

It appears that an emitter-coupled BJT amplifier pair forms a very good differential amplifier with the following properties:

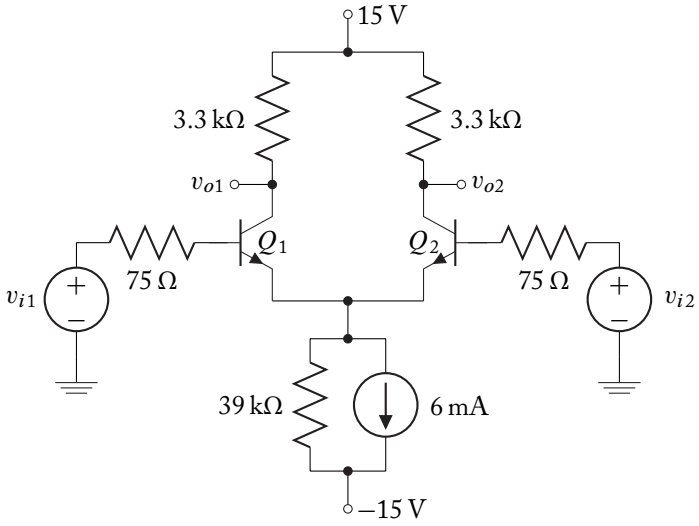
$$\begin{aligned} &\text{Gain:} \quad A_{VD} = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = \frac{-h_{fe}R_c}{h_{ie} + 1/2\{R_{i1} + R_{i2}\}} \\ &\text{Input Resistance:} \quad R_i \approx 2h_{ie} + R_{i2} \\ &\text{Output Resistance:} \quad R_o = R_c. \end{aligned}$$

Example 6.4

Determine the differential voltage gain for the given circuit. Assume identical BJTs with

$$\beta_F = 120.$$

[15] This expression is exactly twice that derived in Chapter 1 (Book 1). The difference is due to the differential nature of the output of this amplifier compared to the single-sided output of an OpAmp. The difference also applies to the common-mode gain: hence the CMRR of the amplifier is unchanged.



Solution:

The output resistance of the current source is much large than either of the output resistances of the sources, thus

$$I_C \approx \frac{\alpha_F}{2}\left(I_{EE} + \frac{V_{EE} - V_{BE(on)}}{R_{EE}}\right)$$

$$I_C \approx 0.4959\left(6\,\text{m} + \frac{14.3}{39\,\text{k}}\right) = 3.157\ \text{mA}.$$

A check of V_{CE} must be made:

$$V_{CE} = V_C - V_E = (15 - I_C R_c) - (0 - I_B R_i - V_{BE(on)}) = 4.58 - (-.702) = 5.28\,\text{V}.$$

The BJT is in the forward-active region. The significant BJT parameters are then:

$$h_{fe} = 120 \quad \text{and} \quad h_{ie} = 996.5\,\Omega.$$

The differential gain is given by:

$$A_{VD} = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = \frac{-h_{fe} R_c}{h_{ie} + 1/2\,\{R_{i1} + R_{i2}\}} = \frac{-120\,(3.3\,\text{k})}{996.5 + 75} = -370.$$

Example 6.5

Use exact expressions for currents, resistances and gains in the circuit of Example 6.4 to determine the single and differential voltage gains and the CMRR for the circuit.

Solution:

The exact collector current expression is:

$$I_C = \beta_F \left(\frac{V_{EE} + I_{EE} R_{EE} - V_{BE(on)}}{2\,(\beta_F + 1)\, R_{EE} + R_i} \right) = 120 \left(\frac{15 + 234 - 0.7}{2\,(121)\,39\,\text{k} + 75} \right) = 3.157\ \text{mA}.$$

There is no significant change from the approximate value of the previous example: the BJTs are in the forward-active region. The BJT h-parameters are:

$$h_{fe} = 120 \quad \text{and} \quad h_{ie} = 996.5\,\Omega.$$

The resistance R_2 is given by:

$$R_2 = \frac{h_{ie} + R_{i2}}{h_{fe} + 1} = \frac{996.5 + 75}{121} = 8.86\ \Omega$$

and the resistance R_1 is

$$R_1 = h_{ie} + (h_{fe} + 1)(R_{EE} // R_2) = 996.5 + (121)(39\,\text{k} // 8.86) = 2.068\,\text{k}\Omega.$$

The load resistance for the common-collector stage is given by:

$$R_E = R_{EE} // R_2 = 8.8535\,\Omega.$$

Which leads to the gain expressions:

$$A_{V1} = \frac{-120(3.3\,\text{k})}{2.068\,\text{k}} \left(\frac{2.068\,\text{k}}{2.068\,\text{k} + 75} \right) = -184.807$$

$$A_{V2} = -A_{V1} \left(\frac{2.068\,\text{k} - 996.5}{996.5 + 75} \right) = 184.768.$$

The total transfer relationships can then be written as:

$$v_{o1} = -184.807 v_{i1} + 184.768 v_{i2} \quad \text{and} \quad v_{o2} = 184.768 v_{i1} - 184.807 v_{i2}.$$

The differential gain is given by:

$$v_{od} = v_{o1} - v_{o2} = -369.575(v_{i1} - v_{i2})$$

and the common-mode gain is

$$v_{oc} = \frac{v_{o1} + v_{o2}}{2} = -0.039234 \left(\frac{v_{i1} + v_{i2}}{2} \right).$$

Which yields a common-mode rejection ratio

$$\text{CMRR} = 20 \log_{10} \left| \frac{-369.575}{-0.039234} \right| = 79.5\ \text{dB}.$$

6.3.2 SOURCE-COUPLED PAIRS

Source-coupled amplifier pairs are the Field Effect Transistor equivalent of emitter-coupled BJT amplifiers. The basic topology is shown in Figure 6.13.[16] As in the emitter-coupled pair, it is important that the two field-effect transistors have similar properties. Similarly, the drain resistances, R_d, are to have similar values and may be composed of simple discrete resistors or active loads. The bias network is almost always a current source, but is shown here as its Norton equivalent.

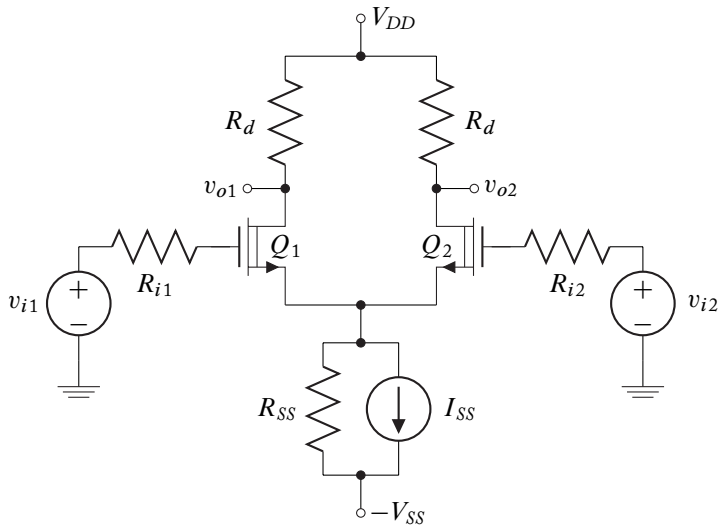


Figure 6.13: A typical source-coupled pair circuit diagram.

DC Analysis of the Source-Coupled Pair

DC analysis of FET circuits is inherently more complicated than BJT circuits due to the highly non-linear large-signal behavior of FETs. Thus, a closed-form expression for the quiescent FET drain current is not easily derived. If, however, the circuit is truly symmetric, the DC analysis can be accomplished through the use of a "half-circuit" as shown in Figure 6.14.

Half-circuit analysis uses the property that the drain currents for the two FETs are identical: thus the effect of the Norton source on *one* of the FETs appears to be modified. This modification changes the apparent Norton source: the value of the Norton current is halved and the Norton resistance appears to be doubled. The drain current and gate-source voltage for this single FET quiescent equivalent circuit can be obtained using the half-circuit quiescent equivalent and the techniques outlined in Chapter 4 (Book 1). These derived quiescent conditions and the FET

[16]Here the FETs are shown as depletion mode n-channel FETs for simplicity. Any other type of FET can be used in a source-coupled pair. Many commercially available OpAmps use source-coupled JFETs or MOSFETs for differential amplifier input stages.

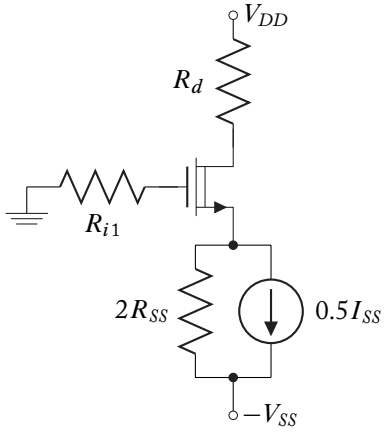


Figure 6.14: A half-circuit equivalent for quiescent condition calculation.

characteristic parameters lead directly to the small-signal FET parameters:

$$g_m = \begin{cases} \dfrac{2\ I_D}{(V_{GS} - V_{PO})} \\ \text{or} \\ 2\ \mathrm{K}\,(V_{GS} - V_T) \end{cases} \qquad r_d = \left| \frac{V_A}{I_D} \right| . \tag{6.67}$$

AC Analysis of the Source-Coupled Pair

As in the emitter-coupled pair, a good method of AC analysis is through the use of superposition. The AC equivalent circuit for zero v_{i2} is shown in Figure 6.15.

The gain path to v_{o1} is a common-source (with a source resistor) amplifier stage, while the gain path to v_{o2} is a two-stage cascaded amplifier, a common-drain stage followed by a common-gate stage. Table 5.13 provides small-signal amplifier performance parameters to guide the AC analysis of this circuit. Two derived input resistances aid in calculations. The resistance, R_2, is the input resistance of a common-gate amplifier:

$$R_2 = \frac{r_d + R_d}{1 + g_m r_d} \tag{6.68}$$

R_1 is the input resistance of a common-drain amplifier:

$$R_1 \approx \infty.$$

Typically, the biasing current source output resistance, R_{SS}, is much greater than the input resistance to the common-gate stage, R_2 (a very small value). This relationship leads to a common approximation, $R_S = R_{SS} // R_2 \approx R_2$.

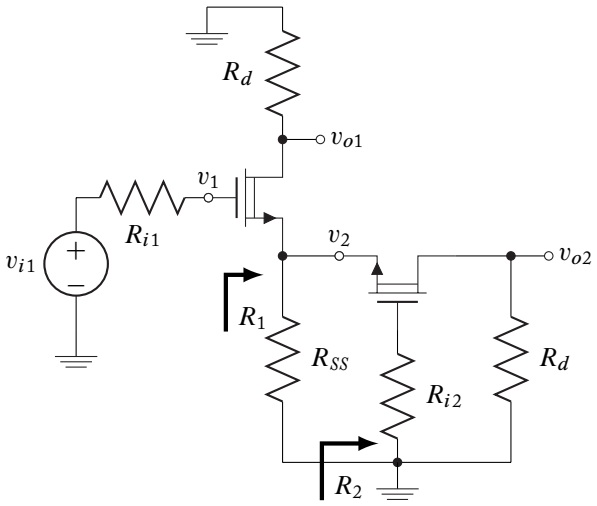


Figure 6.15: AC equivalent circuit for source-coupled pair (single input source).

The voltage gain to each of the output terminals can now be easily determined. The voltage gain to the v_{o1} terminal is simply the product of a common-source amplifier gain and a voltage division:

$$A_{V1} = \frac{v_{o1}}{v_{i1}} = \left(\frac{v_{o1}}{v_1}\right)\left(\frac{v_1}{v_{i1}}\right)$$
$$A_{V1} = \left(\frac{-g_m r_d R_d}{r_d + R_d + (1 + g_m r_d) R_S}\right)\left(\frac{1}{1}\right) \approx \frac{-g_m r_d R_d}{2(r_d + R_d)}. \tag{6.69}$$

The voltage gain to the v_{o2} terminal is the product of a common-base amplifier gain, a common-collector amplifier gain, and a voltage division:

$$A_{V2} = \frac{v_{o2}}{v_{i1}} = \left(\frac{v_{o2}}{v_2}\right)\left(\frac{v_2}{v_1}\right)\left(\frac{v_1}{v_{i1}}\right)$$
$$A_{V2} = \left(\frac{(1 + g_m r_d) R_d}{r_d + R_d}\right)\left(\frac{g_m r_d R_S}{r_d + R_d + (1 + g_m r_d) R_S}\right)\left(\frac{1}{1}\right)$$

rearranging terms leads to:

$$A_{V2} = \left(\frac{g_m r_d R_d}{r_d + R_d + (1 + g_m r_d) R_S}\right)\left(\frac{(1 + g_m r_d) R_S}{r_d + R_d}\right) = -A_{V1}\left(\frac{(1 + g_m r_d) R_S}{r_d + R_d}\right) \tag{6.70}$$

or, when the approximate value of R_S is inserted,

$$A_{V2} \approx -A_{V1}\left(\frac{(1+g_m r_d)\left(\dfrac{r_d+R_d}{1+g_m r_d}\right)}{r_d+R_d}\right) = -A_{V1}. \tag{6.71}$$

Once again, the two gain expressions (given in Equations (6.69) and (6.71)) are equal in magnitude:[17]

$$A_{V2} = -A_{V1} = A$$

where

$$A \approx \frac{g_m r_d \mathrm{R_d}}{2\,(r_d+R_d)}. \tag{6.72}$$

Application of symmetry to this circuit leads to similar expressions for the voltage gains to each output from input v_{i2} when v_{i1} is set to zero value.

$$\frac{v_{o1}}{v_{i2}} = A \quad \text{and} \quad \frac{v_{o2}}{v_{i2}} = -A. \tag{6.73}$$

The total output voltage expressions can then be expressed as a superposition of the results of the derivations:

$$\begin{aligned} v_{o1} &= -Av_{i1} + Av_{i2} \\ v_{o2} &= Av_{i1} - Av_{i2}. \end{aligned} \tag{6.74}$$

The differential output, v_{od}, depends only on the differential input:

$$v_{od} = v_{o1} - v_{o2} = (-Av_{i1} + Av_{i2}) - (Av_{i1} - Av_{i2}) = -2A(v_{i1} - v_{i2}) \tag{6.75}$$

$$v_{od} = \frac{-g_m r_d R_d}{(r_d+R_d)}\,(v_{i1} - v_{i2})\,. \tag{6.76}$$

The common output, v_{oc}, is approximately zero:

$$v_{oc} = 1/2(v_{o1} + v_{o2}) = 1/2\{(-Av_{i1} + Av_{i2}) + (Av_{i1} - Av_{i2})\} \approx 0. \tag{6.77}$$

If it is assumed that R_{SS} is large with respect to R_2, the output resistance at the output terminal of the FET is given by:

$$R_o \approx 2r_d + R_d. \tag{6.78}$$

[17]The equivalence is true only for the approximation $R_S = R_{SS}//R_2 \approx R_2$. The gain expressions of Equations (6.69) and (6.70) are exact.

The total output resistance (including effects of the load resistance R_d) is given by:

$$R_o \approx R_d \left(1 - \frac{R_d}{2\,(r_d + R_d)}\right). \tag{6.79}$$

A source-coupled FET amplifier pair also forms a very good differential amplifier with the following properties:

$$\begin{aligned}
&\text{Gain:} \qquad A_{VD} = \frac{v_{o1} - v_{o2}}{v_{i1} - v_{i2}} = \frac{-g_m r_d R_d}{(r_d + R_d)} \\
&\text{Input Resistance:} \quad R_i \approx \infty \\
&\text{Output Resistance:} \quad R_o \approx R_d \left(1 - \frac{R_d}{2\,(r_d + R_d)}\right).
\end{aligned}$$

Example 6.6

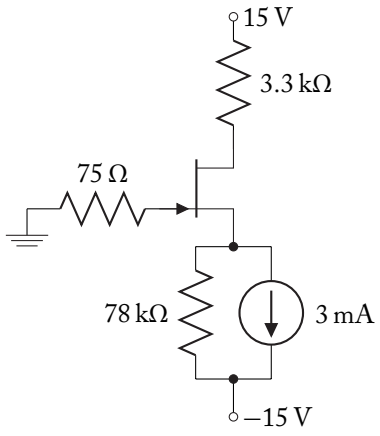
The Source-coupled amplifier of Figure 6.13 is constructed with two identical JFETs with properties:

$$V_{PO} = -4\,\text{V} \quad I_{DSS} = 8\,\text{mA} \quad V_A = 160\,\text{V}$$

and circuit parameters:

$$\begin{aligned}
V_{DD} = V_{SS} &= +15\,\text{V} \qquad I_{SS} = 6\,\text{mA} \\
R_{SS} &= 39\,\text{k}\Omega \qquad R_d = 3.3\,\text{k}\Omega.
\end{aligned}$$

Determine the circuit performance parameters and CMRR.



Solution

The DC analysis uses the half-circuit analysis technique to obtain values of I_D and V_{GS}. The two significant equations are:

$$I_D = 8\,\text{mA}\left(1 + \frac{V_{GS}}{4}\right)^2 \quad \text{and} \quad I_D = \frac{15 - V_{GS}}{78\,\text{k}} + 3\,\text{mA}.$$

The solutions to the above are:

$$I_D = 3.2111\,\text{mA} \quad \text{and} \quad V_{GS} = -1.4658\,\text{V}$$

V_{DS} must be checked:

$$V_{DS} = 15 - (3.2111\,\text{m})\,(3.3\,\text{k}) - 1.4658 = 2.938 \geq -1.4658 + 4 = 2.534.$$

The JFET is in the saturation region. The AC small-signal parameters can now be determined:

$$g_m = \frac{2\,(3.2111\,\text{m})}{2.5342} = 2.534\,\text{mA/V} \qquad r_d = \left|\frac{-160}{3.2111\,\text{m}}\right| = 49.83\,\text{k}\Omega.$$

AC analysis can now proceed.

$$A_{VD} = \frac{-g_m r_d R_d}{(r_d + R_d)} = \frac{-2.534\,\text{m}\,(49.83\,\text{k})\,(3.3\,\text{k})}{(49.83\,\text{k} + 3.3\,\text{k})} = -7.843$$

$$R_o \approx R_d\left(1 - \frac{R_d}{2\,(r_d + R_d)}\right) = 3.3\,\text{k}\left(1 - \frac{3.3\,\text{k}}{2\,(49.83\,\text{k} + 3.3\,\text{k})}\right) = 3.197\,\text{k}\Omega.$$

CMRR calculations need the more exact expressions for resistances and gain. The resistance R_2 is given by:

$$R_2 = \frac{r_d + R_d}{1 + g_m r_d} = \frac{49.83\,\text{k} + 3.3\,\text{k}}{1 + 126.27} = 417.45\ \Omega$$

and the total resistance seen by the source of the FETs is:

$$R_S = R_{SS}//R_2 = 39\,\text{k}//417.45 = 413.03\,\Omega.$$

The two voltage gain expressions (using exact values of R_S) are given by Equation (6.69):

$$A_{V1} = \left(\frac{-g_m r_d R_d}{r_d + R_d + (1 + g_m r_d)\,R_S}\right)$$

$$= \left(\frac{-126.27\,(3.3\,\text{k})}{49.83\,\text{k} + 3.3\,\text{k} + (1 + 126.27)\,413.03}\right) = -3.94238$$

and Equation (6.70):

$$A_{V2} = -A_{V1}\left(\frac{(1+g_m r_d)\,R_S}{r_d + R_d}\right) = -3.94238\left(\frac{(1+126.27)\;413.03}{49.83\,\text{k} + 3.3\,\text{k}}\right) = 3.90064.$$

The differential-mode gain is:

$$A_{DM} = A_{V1} - A_{V2} = -7.843$$

and the common-mode gain is:

$$A_{CM} = A_{V1} + A_{V2} = -0.04175$$

for a CMRR of

$$CMRR = 20\log_{10}\left|\frac{-7.84302}{-0.0417465}\right| = 45.5\text{ dB}.$$

6.3.3 VARIATIONS ON THE THEME

In an effort to improve the various performance characteristics of emitter-coupled and source-coupled amplifiers, designers often change the circuit topology while keeping its basic characteristics. Two common techniques for altering circuit performance are:

- Including a resistor between the emitter or source terminal and the common terminal
- Using a compound transistor (Darlington, etc.) instead of a single transistor

Additional resistors have the effect of increasing the range of input voltages over which the amplifier is linear and increases the input resistance of emitter-coupled amplifiers. Compound transistors can have a variety of effects. Figure 6.16 shows a simplified schematic of the input stage of an OpAmp that uses compound Darlington transistors and additional emitter resistors to alter performance characteristics.

While the circuit of Figure 6.16 indicates a multiple BJT differential amplifier, the compound transistors are not limited to BJTs. BiFET and BiCMOS technologies allow for the mixing of transistor types in the differential pair as long as the circuit remains symmetric. Analysis of such amplifiers follows the same basic techniques as have been demonstrated in this section. The compound transistor parameters rather than single transistor parameters are used and appropriate resistances (R_1 and/or R_2 in the previous derivations) are modified to reflect any additional emitter or source resistors.

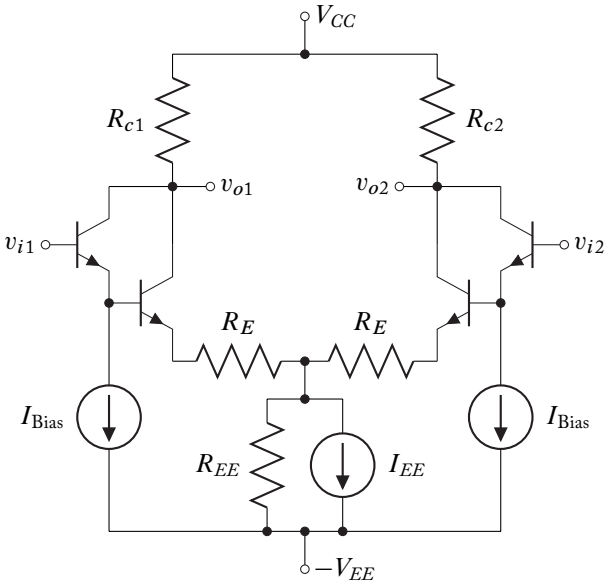


Figure 6.16: Simplified input stage schematic: LM318 OpAmp.

6.3.4 SUMMARY

The basic performance characteristics of basic emitter-coupled and source-coupled amplifiers are summarized in Table 6.1.

Table 6.1: Summary of differential pair amplifier properties[18]

	Emitter-Coupled	Source-Coupled
Differential Voltage Gain	$\dfrac{-h_{fe}R_c}{h_{ie}+(R_{i1}+R_{i2})/2}$	$\dfrac{-g_m r_d R_d}{r_d+R_d}$
Input Resistance	$2h_{ie}+R_i$	$\approx\infty$
Output Resistance[18]	$\approx\infty$ $\approx R_c$	$\approx 2r_d+R_d$ $\approx R_D\left(1-\dfrac{R_d}{2(r_d+R_d)}\right)$

[18]The upper row is output resistance measured at the output terminal of the transistor. The lower line includes the effect of the load resistance R_c or R_d.

6.4 TRANSISTOR CURRENT SOURCES

Current sources may be used to bias the transistor circuit in the forward active region for a small-signal amplifier. The biasing schemes explored thus far apply a voltage across the base-emitter junction of the BJT or the gate-source of the FET. Current source biasing may be used in lieu of a base or gate resistor bias network to set the quiescent collector or drain current, and is the preferred method for biasing differential amplifiers. Bias networks in integrated circuits most often depend on current sources.

6.4.1 SIMPLE BIPOLAR CURRENT SOURCE

A simple BJT current source that delivers an approximately constant collector current I_C is shown in Figure 6.17. For this current source to be operational, the collector voltage of the BJT must be sufficiently more positive than the emitter voltage such that the transistor operates in the forward active region. The constant current is supplied by the collector of the transistor.

The transistor collector current can be obtained, by applying the node voltage method at V_B; that is, by summing the currents at the base of Q_1

$$0 = I_1 + I_2 + I_B. \tag{6.80}$$

Using Kirchhoff's Voltage Law around the base-emitter loop yields an expression for V_B,

$$V_B = I_3 R_3 + V_{BE} - V_{EE}. \tag{6.81}$$

The current I_1 can be expressed in terms of I_3 by substituting Equation (6.81) for the base voltage,

$$I_1 = \frac{V_B}{R_1} = \frac{I_3 R_3 + V_{BE} - V_{EE}}{R_1}. \tag{6.82}$$

The current I_2 is found in a similar manner,

$$I_2 = \frac{V_B - 2V_d + V_{EE}}{R_2} = \frac{I_3 R_3 + V_{BE} - 2V_d}{R_2}, \tag{6.83}$$

where V_d is the voltage drop across each of the diodes D_1 and D_2. The base current is simply,

$$I_B = \frac{I_3}{\beta_F + 1}. \tag{6.84}$$

Substitution of Equations (6.82) to (6.84) into (6.80) yields an expression in terms of the emitter current I_3,

$$0 = \frac{I_3 R_3 + V_{BE} - V_{EE}}{R_1} + \frac{I_3 R_3 + V_{BE} - 2V_d}{R_2} + \frac{I_3}{\beta_F + 1}. \tag{6.85}$$

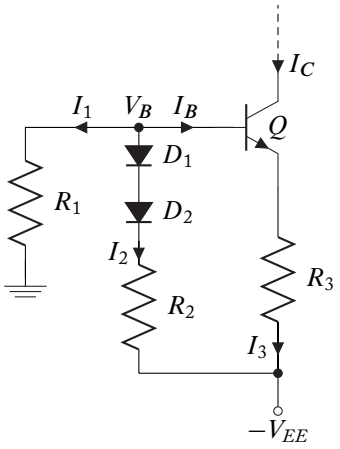


Figure 6.17: Simple BJT current source.

Solving for I_3 in Equation (6.85),

$$I_3 = \frac{R_2(V_{EE} - V_{BE}) + R_1\,(2V_d - V_{BE})}{R_2R_3 + R_1R_3 + \dfrac{R_1R_2}{(\beta_F + 1)}}. \tag{6.86}$$

The collector current is found to be,

$$\begin{aligned} I_C &= \frac{\beta_F}{\beta_F + 1}\left[\frac{R_2(V_{EE} - V_{BE}) + R_1\,(2V_d - V_{BE})}{R_2R_3 + R_1R_3 + \dfrac{R_1R_2}{(\beta_F + 1)}}\right] \\ &= \beta_F\left[\frac{R_2(V_{EE} - V_{BE}) + R_1\,(2V_d - V_{BE})}{(\beta_F + 1)\,(R_2R_3 + R_1R_3) + R_1R_2}\right]. \end{aligned} \tag{6.87}$$

An additional benefit of using diodes this and similar biasing networks is the reduction of collector current dependence on base-emitter temperature. The reduction of collector current dependence on the BJT junction temperature increases the stability of the operating point.

6.4.2 CURRENT MIRROR

The simple current source in Figure 6.17 is useful but requires two diodes, one transistor, and three resistors to configure. A two transistor current source, which use fewer components (in particular, resistors) is shown in Figure 6.18. This configuration is commonly called a current mirror,

The constant current is supplied from the collector of Q_2. The base-collector voltage of Q_1 is equal to zero ensuring that the BJT is operating in the forward-active region. This connection

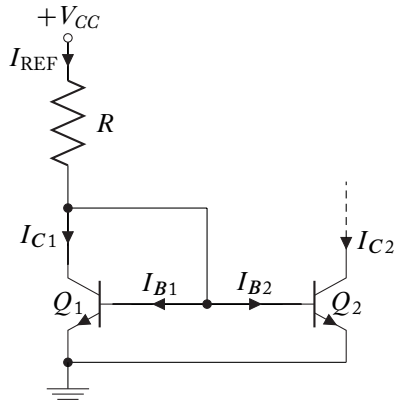


Figure 6.18: The simple BJT current mirror.

is referred to as a diode-connected BJT. If the transistors are identical, both Q_1 and Q_2 have the same base-emitter voltages, therefore $I_{B1} = I_{B2}$ and $I_{C1} = I_{C2}$ since $\beta_{F1} = \beta_{F2} = \beta_F$. Applying Kirchhoff's Current Law at the collector node of Q_1,

$$I_{REF} = I_{C1} + I_{B1} + I_{B2} = I_{C1} + \frac{2I_{C1}}{\beta_F} = I_{C1}\left(1 + \frac{2}{\beta_F}\right). \tag{6.88}$$

Therefore, the collector current of Q_2 is,

$$I_{C2} = I_{C1} = \frac{I_{REF}}{1 + \dfrac{2}{\beta_F}}. \tag{6.89}$$

Solving for I_{REF} in terms of the applied voltage V_{CC} and resistance R,

$$I_{REF} = \frac{V_{CC} - V_\gamma}{R}, \tag{6.90}$$

since $V_{CE1} = V_\gamma$.

Substituting Equation (6.90) into (6.89) and solving for I_{C1},

$$I_{C1} = \frac{V_{CC} - V_\gamma}{\left(1 + \dfrac{2}{\beta_F}\right) R}. \tag{6.91}$$

So the Q_2 collector current (constant current) is,

$$I_{C2} = I_{C1} = \frac{V_{CC} - V_\gamma}{\left(1 + \dfrac{2}{\beta_F}\right) R}. \tag{6.92}$$

I_{C2} is also dependent on V_{CE2}. For a constant base current, the collector current will increase slowly as the collector-emitter voltage increases. In the current mirror of Figure 6.18, $V_{CE2} \geq V_{CE1}$ since $V_{CE1} = V_{BE1}$. The value of V_{CE2} depends on the bias voltage at the collector of Q_2. Typically, $V_{CE2} \gg V_{CE1}$. Depending on the quiescent conditions of Q_2, I_{C2} may be up to 10% larger than I_{C1}.

Stability is an important parameter of constant current sources. Variations in parameter values will cause an undesirable fluctuation in I_{C2}. The stability factors defined in Section 3.7 (Book 1) are,

$$S_I = \frac{\partial I_{C2}}{\partial I_{CO}}, \quad S_V = \frac{\partial I_{C2}}{\partial V_{BE}}, \quad S_\beta = \frac{\partial I_{C2}}{\partial \beta_F}. \tag{6.93}$$

Using Equation (6.92)

$$S_I = \frac{\partial}{\partial I_{CO}} \left[\frac{V_{CC} - V_\gamma}{\left(1+\frac{2}{\beta_F}\right) R} + (\beta_F+1)\, I_{CO} \right] = (\beta_F+1)\,, \tag{6.94}$$

$$S_V = \frac{\partial}{\partial V_{BE}} \left[\frac{V_{CC} - V_{BE}}{\left(1+\frac{2}{\beta_F}\right) R} \right] = -\frac{1}{\left(1+\frac{2}{\beta_F},\right) R} \tag{6.95}$$

and

$$S_\beta = \frac{\partial}{\partial \beta_F} \left[\frac{V_{CC} - V_\gamma}{\left(1+\frac{2}{\beta_F}\right) R} \right] = \frac{2(V_{CC} - V_\gamma)}{R(\beta_F + 2)^2}. \tag{6.96}$$

By increasing R, better stability against variations in base-emitter voltage and quiescent point shifts due to varying β_F can be obtained. The advantage of the current mirror in Figure 6.18 is the reduction in the number of resistors that makes the circuit more applicable to integrated circuits.

6.4.3 CURRENT MIRROR WITH ADDITIONAL STABILITY

A third transistor can be added to gain more stability in the quiescent point. Using three identical transistors, Q_3 in a common collector configuration at the base of Q_1 and Q_2 is used to provide additional stability. The three transistor current source is shown in Figure 6.19.

Since the base-emitter voltages of Q_1 and Q_2 are identical, $I_{B1} = I_{B2}$ and $I_{C1} = I_{C2}$ with $\beta_{F1} = \beta_{F2} = \beta_{F3} = \beta_F$. The emitter current of Q_3 is,

$$-I_{E3} = I_{B1} + I_{B2} = \frac{I_{C1}}{\beta_F} + \frac{I_{C2}}{\beta_F} = \frac{2I_{C2}}{\beta_F}. \tag{6.97}$$

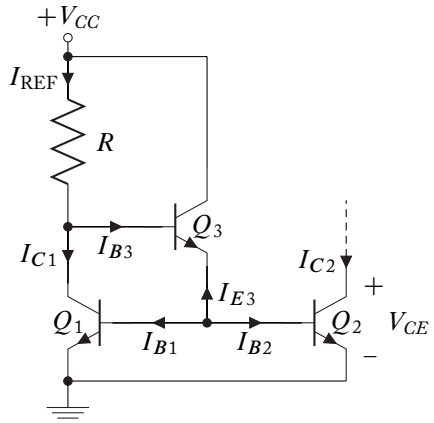


Figure 6.19: Three transistor current mirror.

The base current of Q_3 is therefore,

$$I_{B3} = \frac{-I_{E3}}{\beta_F + 1} = \frac{2I_{C2}}{\beta_F\,(\beta_F + 1)}. \tag{6.98}$$

Using Equation (6.98) and the fact that $I_{C1} = I_{C2}$, the reference current can be found,

$$I_{REF} = I_{C1} + I_{B3} = I_{C2} + \frac{2I_{C2}}{\beta_F\,(\beta_F + 1)}. \tag{6.99}$$

The reference current is found by applying Kirchhoff's Voltage Law from I_{REF} through the base-emitter junctions of Q_3 and Q_1,

$$I_{REF} = \frac{V_{CC} - V_{BE1} - V_{BE3}}{R} = \frac{V_{CC} - 2V_\gamma}{R}. \tag{6.100}$$

Rearranging Equation (6.99) to solve for I_{C2} using the expression for I_{REF} in Equation (6.100),

$$I_{C2} = \frac{I_{REF}}{1 + \dfrac{2}{\beta_F\,(\beta_F + 1)}} = \frac{V_{CC} - 2V_\gamma}{R\left[1 + \dfrac{2}{\beta_F\,(\beta_F + 1)}\right]}. \tag{6.101}$$

The current gain stability factor is found by differentiating Equation (6.101) with respect to β_F,

$$\begin{aligned} S_\beta &= \frac{\partial}{\partial \beta_F}\left[\frac{V_{CC} - 2V_\gamma}{R\left[1 + \dfrac{2}{\beta_F\,(\beta_F + 1)}\right]}\right] \\ &= \frac{2\,(2\beta_F + 1)\,(V_{CC} - 2V_\gamma)}{R[\beta_F\,(\beta_F + 1) + 2]^2} = \frac{2I_{REF}\,(2\beta_F + 1)}{[\beta_F\,(\beta_F + 1) + 2]^2}. \end{aligned} \tag{6.102}$$

Recall that in the two transistor current mirror in Section 6.4.2, the β stability factor was approximately proportional to β_F^{-2}. For the three transistor current mirror, the β stability factor is approximately proportional to β_F^{-3}. Therefore, the stability of the three transistor current mirror has greater stability than the two transistor current mirror by a factor of β_F . This indicates that the collector current is tightly bound to the desired value caused by operating temperature swings or through parameter changes as a result of interchanging individual transistors with slightly different characteristics, which is commonly encountered when mass producing BJT circuits.

6.4.4 WILSON CURRENT SOURCE

The Wilson current source is used when low sensitivity to transistor base currents is desired and is shown in Figure 6.20. The transistors are again assumed to be identical for this analysis. Applying Kirchhoff's Current Law to the collector of Q_3 yields and expression for the emitter current of Q_2,

$$-I_{E2} = I_{B1} + I_{B3} + I_{C3} = \frac{I_{C1}}{\beta_F} + I_{C3}\left(1 + \frac{1}{\beta_F}\right). \tag{6.103}$$

However, since Q_1 and Q_3 are identical and have identical values of base-emitter voltage, the collector currents are also equal ($I_{B1} = I_{B3}$ and $I_{C1} = I_{C3}$ with $\beta_{F1} = \beta_{F2} = \beta_{F3} = \beta_F$). Therefore, Equation (6.103) can be put in terms of only I_{C3},

$$-I_{E2} = I_{C3}\left(1 + \frac{2}{\beta_F}\right). \tag{6.104}$$

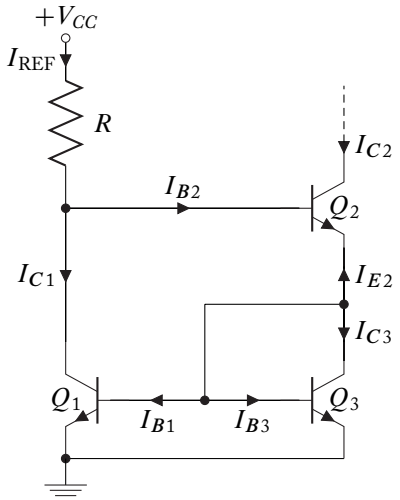


Figure 6.20: Wilson current mirror.

From Equation (6.104) the collector current of Q_2 can be determined,

$$I_{C2} = -I_{E2}\frac{\beta_F}{\beta_F+1} = I_{C3}\left(1+\frac{2}{\beta_F}\right)\left(\frac{\beta_F}{\beta_F+1}\right). \tag{6.105}$$

Applying Kirchhoff's Current Law at the base of Q_2,

$$I_{REF} = I_{C1} + I_{B2} = I_{C1} + \frac{I_{C2}}{\beta_F}. \tag{6.106}$$

But since the transistors are identical, $I_{C1} = I_{C3}$ so, rearranging Equation (6.106),

$$I_{C3} = I_{REF} - \frac{I_{C2}}{\beta_F} \tag{6.107}$$

Substituting Equation (6.107) into (6.105),

$$I_{C2} = \left(I_{REF} - \frac{I_{C2}}{\beta_F}\right)\left(1 + \frac{2}{\beta_F}\right)\left(\frac{\beta_F}{\beta_F+1}\right). \tag{6.108}$$

Rearranging Equation (6.108) yields the Q_2 collector current in terms of the reference current,

$$I_{C2} = I_{REF}\frac{\beta_F^2 + 2\beta_F}{\beta_F^2 + 2\beta_F + 2} = I_{REF}\left(1 - \frac{2}{\beta_F^2 + 2\beta_F + 2}\right). \tag{6.109}$$

From Equation (6.109) it is apparent that the output current differs from the reference current by a small amount corresponding to approximately $2/\beta_F^2$.

6.4.5 WIDLAR CURRENT SOURCE

In the two and three transistor current mirrors, the load current I_{C2} is approximately equal to the reference current for large β_F. To supply a load current of milliamperes with power supply voltages in the order of 10 V, the reference resistor must be in the several thousands of Ohms. This poses little problem for the designer. However, if the load current is small (in the order of 5 μA), the required reference resistor approaches or exceeds 1 MΩ. In Operational amplifier integrated circuits, the low input current requirement mandates a low bias current for the input emitter-coupled differential amplifier. A resistor of this magnitude is prohibitive in terms of the area that it would require on the chip. It is also difficult to fabricate accurate resistance values on integrated circuit chips.

The load and reference currents can be made to be substantially different by forcing the base-emitter voltages of Q_1 and Q_2 to be unequal in the two transistor current mirror of Figure 6.18. One way to achieve this goal of substantially different load and reference currents is the addition of an emitter resistor to Q_2 as is done in the Widlar current source shown in Figure 6.21. Applying Kirchhoff's Voltage Law to the base-emitter loop of Q_1 and Q_2,

$$0 = V_{BE1} - V_{BE2} + I_{E2}R_2. \tag{6.110}$$

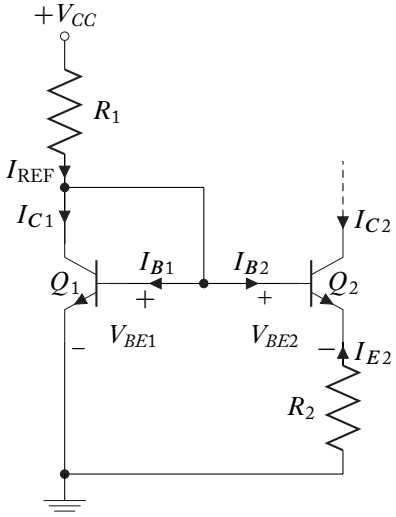


Figure 6.21: The Widlar current source.

The collector currents of Q_1 and Q_2 can be related to the base-emitter voltages by using the Ebers-Moll equation from 3.3b, Chapter 3 (Book 1)

$$I_C = -I_{CS}\left(e^{\frac{V_{BC}}{\eta V_t}} - 1\right) + \alpha_F I_{ES}\left(e^{\frac{V_{BE}}{\eta V_t}} - 1\right). \tag{6.111}$$

Equation (3.8, Chapter 3 (Book 1)) gives the saturation current values:

$$\alpha_F I_{ES} = I_S. \tag{6.112}$$

For a transistor operating in the forward active region, $V_{BC} \leq 0$. Therefore, Equation (6.111) simplifies to,

$$I_C \approx I_S\left(e^{\frac{V_{BE}}{\eta V_t}} - 1\right). \tag{6.113}$$

So the base-emitter voltage of a transistor is,

$$V_{BE} = \eta V_t \ln\left(\frac{I_C}{I_S} + 1\right). \tag{6.114}$$

Using Equation (6.114), the loop equation of Equation (6.110) is

$$\begin{aligned} 0 &= \eta_1 V_t \ln\left(\frac{I_{C1}}{I_{S1}}+1\right) - \eta_2 V_t \ln\left(\frac{I_{C2}}{I_{S2}}+1\right) + I_{E2}R_2 \\ &= \eta_1 V_t \ln\left(\frac{I_{C1}}{I_{S1}}+1\right) - \eta_2 V_t \ln\left(\frac{I_{C2}}{I_{S2}}+1\right) - \frac{\beta_F+1}{\beta_F} I_{C2}R_2. \end{aligned} \tag{6.115}$$

If the transistors are identical, $I_{S1} = I_{S2}$ and $\eta_1 = \eta_2$. Then Equation (6.115) may be simplified as,

$$\eta V_t \ln\left(\frac{I_{C1}+I_S}{I_{C2}+I_S}\right) = \frac{\beta_F+1}{\beta_F} I_{C2}R_2. \tag{6.116}$$

Since the saturation current is very small compared to the collector current for BJTs in the forward active region,

$$\eta V_t \ln\left(\frac{I_{C1}}{I_{C2}}\right) = \frac{\beta_F+1}{\beta_F} I_{C2}R_2. \tag{6.117}$$

This is a transcendental function that must be solved by iterative techniques for a given R_2 and I_{C1} (or I_{REF}) to find I_{C2}.

Example 6.7

For the Widlar current source shown in Figure 6.19, the required load current is $I_{C2} = 5\,\mu$A, $I_{C1} = 1$ mA, $V_{CC} = 5$ V, $V_{BE} = 0.7$ V, $V_T = 0.026$ V, $\beta_F = 200$, and $\eta = 1$. Find the two resistance values and the reference current.

Solution:

From Equation (6.117),

$$(0.026)\ln\left(\frac{10^{-3}}{5\times10^{-6}}\right) = \frac{201}{200}\left(5\times10^{-6}\right)R_2,$$

yielding the value

$$R_2 = 27.5\,\text{k}\Omega \approx 27\,\text{k}\Omega.$$

Using Kirchhoff's Current Law at the collector node of Q_1.

$$\begin{aligned} I_{REF} &= I_{C1} + I_{B1} + I_{B2} \\ &= I_{C1}\left(1+\frac{1}{\beta_F}\right) + \frac{I_{C2}}{\beta_F} \\ &= 10^{-3}\left(1+\frac{1}{200}\right) + \frac{5\times10^{-6}}{200} = 1.005\text{ mA}. \end{aligned}$$

The reference resistor is found by applying Kirchhoff's Voltage Law to the collector-base-emitter loop of Q_1,

$$R_1 = \frac{V_{CC} - V_{BE}}{I_{REF}} = \frac{5 - 0.7}{1.005 \times 10^{-3}} = 4.28\ \text{k}\Omega \approx 4.3\ \text{k}\Omega.$$

An example of current source biasing of input emitter-coupled differential amplifier for an OpAmp (μA741) is shown in Figure 6.22. It is a Widlar current source consisting of Q_{12}, Q_{11}, Q_{10}, R_4 and R_5 with the load current taken off of Q_{10}.

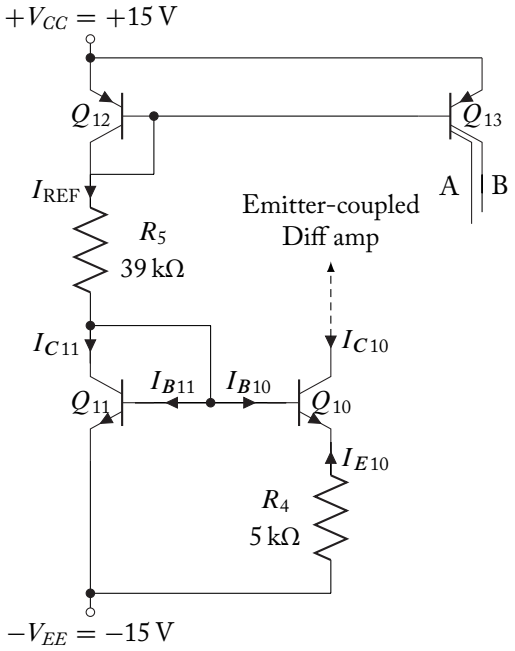


Figure 6.22: Widlar current source used to bias input stage of the μA741 OpAmp.

Analysis of this circuit begins with the reference current, I_{REF}. The reference current is,

$$I_{REF} = \frac{V_{CC} - (-V_{EE}) - V_{BE12} - V_{BE11}}{R_5}$$
$$= \frac{30 - 1.4}{39\,\text{k}} = 0.73\,\text{mA}$$

where $V_{BE12} = V_{BE10} = V_\gamma = 0.7\,\text{V}$.

The output current is found using the transcendental function

$$\eta V_T \ln\left(\frac{I_{C11}}{I_{C10}}\right) = \frac{\beta_F + 1}{\beta_F} I_{C10} R_4 \approx I_{C10} R_4$$

and Kirchhoff's Current Law applied to the collector of Q_{11} as described above. Using $\beta_F = 200$, a math package (MathCAD in this case) determines the output current as

$$I_{C10} = 18.90\,\mu\text{A}.$$

An alternate technique to find the load current is through SPICE simulations. The Multisim output for the Widlar current source in Figure 6.22 is shown in Figure 6.23. Here, the output node was arbitrarily connected to ground and the transistors were assumed to have the following simple parameters:

IS=1pA BF=200 BR=6.

The SPICE simulation produces the same result as the transcendental equations:

$$I_{C10} = 18.87\,\mu\text{A}.$$

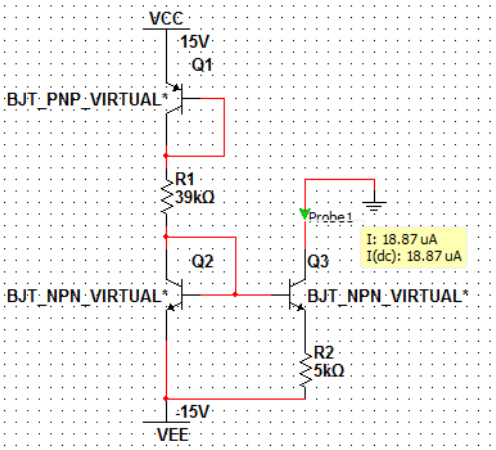


Figure 6.23: SPICE simulation of the OpAmp Widlar current source.

6.4.6 SIMPLE MOSFET CURRENT MIRROR

In MOS integrated circuits, the FETs are biased in their saturation regions through the use of a MOSFET constant current source. A simple enhancement mode NMOSFET current mirror is shown in Figure 6.24. FETs M_1 and M_2 are connected as saturated devices. The reference current I_{REF} and the load current I_{D3} are determined by using the expression for the drain current.

The NMOSFET M_3 is assumed to be in saturation.

$$I_{REF} = K_1(V_{GS1} - V_{T1})^2 = K_2(V_{GS2} - V_{T2})^2 \tag{6.118}$$

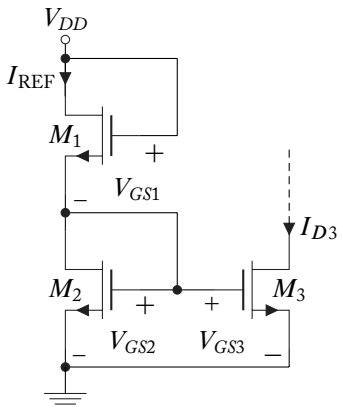


Figure 6.24: Simple enhancement NMOSFET current mirror.

and

$$I_{D3} = K_3(V_{GS3} - V_{T3})^2. \tag{6.119}$$

Apply Kirchhoff's Voltage Law, the gate-source voltage of M_1 is found,

$$V_{GS1} = V_{DD} - V_{GS2}. \tag{6.120}$$

Substituting Equation (6.120) into (6.118)

$$K_1(V_{DD} - V_{GS2} - V_{T1})^2 = K_2(V_{GS2} - V_{T2})^2 \tag{6.121}$$

Rearranging the equation yields,

$$\left[1 + \left(\frac{K_1}{K_2}\right)^{\frac{1}{2}}\right] V_{GS2} = \left(\frac{K_1}{K_2}\right)^{\frac{1}{2}} (V_{DD} - V_{T1}) + V_{T2}. \tag{6.122}$$

Solving for V_{GS2} ,

$$V_{GS2} = \frac{\left(\frac{K_1}{K_2}\right)^{\frac{1}{2}} (V_{DD} - V_{T1}) + V_{T2}}{1 + \left(\frac{K_1}{K_2}\right)^{\frac{1}{2}}}. \tag{6.123}$$

But $V_{GS3} = V_{GS2}$, so the load current I_{D3} is found by substituting Equation (6.123) into Equation (6.119).

Example 6.8

Given an enhancement mode NMOSFET in the circuit of Figure 6.24, find the ratio of the transconductance of the FETs, M_1 and M_2, to achieve a current of

$$I_{D3} = 25\,\mu\text{A}.$$

The other FET parameters are:

$$V_{DD} = 10\,\text{V}, \qquad K_3 = 0.1\,\text{mA/V}^2,$$
$$V_{T1} = V_{T2} = V_{T3} = 1\,\text{V}, \quad I_{REF} = 100\,\mu\text{A}.$$

Solution

Solve for $V_{GS3} = V_{GS2}$ using Equation (6.119)

$$V_{GS2} = V_{GS3} = \sqrt{\frac{I_{D3}}{K_3}} + V_{T3} = \sqrt{\frac{25 \times 10^{-6}}{1 \times 10^{-4}}} + 1 = 1.5\,\text{V}.$$

Rearranging Equation (6.121) yields the required transconductance ratio of M_1 and M_2,

$$\left(\frac{K_2}{K_1}\right) = \left(\frac{V_{DD} - V_{GS2} - V_{T1}}{V_{GS2} - V_{T2}}\right)^2 = \left(\frac{10 - 1.5 - 1}{1.5 - 1}\right)^2 = 255.$$

6.5 ACTIVE LOADS

In integrated circuit amplifiers, transistor current source configurations are often used as active loads. Since small-signal gain in amplifiers is directly proportional to the load resistance, large loads are desired to achieve large gain. However, increasing the load requires that a large power supply voltage must be used in order to keep to transistor in the proper region of operation. The quiescent point will be also be altered. Both of these consequences to the use of a large resistor for a load are undesirable.

Active loads using current source configurations are commonly used to provide the high load required for increasing small-signal gain. The small-signal output resistance of the current source configuration is used as the load to the amplifying circuit. A Norton and Thévenin equivalent model of a transistor current source is shown in Figure 6.25.

For the Norton equivalent model, the analysis and design of current sources, discussed in Section 6.4 using the Ebers-Moll model, is used to determine I_O. The output resistance R_O is found by determining the performing small-signal analysis on the current source. Since a transistor is used in place of a resistor, the load is dependent on both the inherent transistor characteristics and the quiescent point of the circuit. In particular, the Early voltage, V_A, is of great importance when determining the active load of a small-signal transistor amplifier.

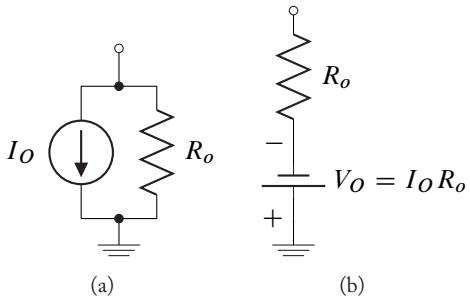


Figure 6.25: (a) Norton and (b) Thévenin equivalent models of constant current sources.

6.5.1 COMMON-EMITTER AMPLIFIER WITH ACTIVE LOAD

A common-emitter amplifier with an active load is shown in Figure 6.26. The active load consists of a simple pnp current mirror. The *pnp* current mirror provides the load for the *npn* BJT common-emitter amplifier. The current mirror also determines the range of bias currents over which the common-emitter will be in the forward active region.

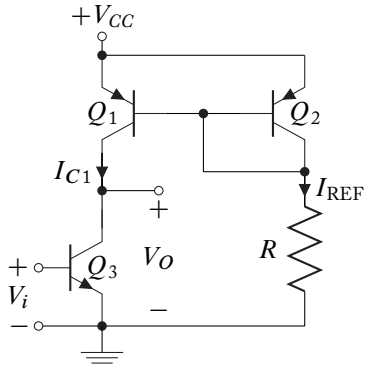


Figure 6.26: Common-emitter amplifier with *pnp* current mirror active load.

The current mirror transistors Q_1 and Q_2 are assumed to be identical. For Q_2 to be in the forward-active region, its collector current and the collector current of the common-emitter BJT, Q_3, must be greater than $I_{C,lower}$, where $I_{C,lower}$ is defined by:

$$I_{C,lower} = \frac{V_{CC} - V_\gamma}{\left(1 + \frac{2}{\beta_{FQ1}}\right) R} \approx I_{REF}. \tag{6.124}$$

This current effectively clips and distorts the output at I_{C3}. From the Ebers-Moll equations and Equation (6.114), the base-emitter bias voltage of Q_3 required to establish this lower current limit of operation is,

$$V_{BE3(lower)} = \eta V_t \ln\left(\frac{I_{C3,lower}}{I_{S1}} + 1\right). \tag{6.125}$$

Therefore, the input voltage V_i must exceed $V_{BE3,lower}$ for operation of Q_3 in the forward-active region.

The characteristic curve of the active load transistor Q_1 superimposed on the set of output characteristic curves for Q_3 is shown in Figure 6.27. The *pnp* BJT, Q_1, acts as a load line of resistance h_{oe}^{-1} on the collector of the common-emitter configured *npn* transistor Q_3. Since the collector current is small, the load is very large. If a resistive load was used instead of an active load, the circuit would require a very large power supply voltage to establish on end of the resistive load line. The active load line formed by Q_1 transitions from the cut-off to forward active region at $I_{C1} = I_{C,lower}$. The upper limit of amplifier operation for Q_3 is established when the active load line crosses the point where Q_3 saturates. This point establishes the upper limit, $I_{C,upper}$, on Q_3, and can be approximated as described in Equation (6.126).

$$I_{C,upper} = I_{C,lower} + \frac{V_{CC} - V_{CE3(sat)}}{1/h_{oe1}}. \tag{6.126}$$

The corresponding base-emitter voltage of Q_3 is,

$$V_{BE3(upper)} = \eta V_t \ln\left(\frac{I_{C,upper}}{I_{S1}} + 1\right) \tag{6.127}$$

A plot of the Q_3 collector voltage and collector current of Q_3 as a function of input voltage is shown in Figure 6.28. The Q_3 collector voltage versus the input voltage in Figure 6.28 is a transfer characteristic of the common-emitter amplifier.

Small-signal analysis is used to determine the common-emitter load. The AC and small-signal models of the common-emitter circuit in Figure 6.26 is shown in Figure 6.29. To find the Thévenin resistance, R_{TH} , of the *pnp* current mirror, the resistance looking into the nodes C_3, C_1, and E_1 is found. For the common-emitter circuit in Figure 6.26, the load (Thévenin) resistance is $R_O = h_{oe}^{-1}$. From Equation (5.34), the output resistance is

$$R_O = \frac{1}{h_{oe1}} = \frac{|V_{A1}|}{I_{C1}}, \tag{6.128}$$

where V_{A1} is the Early voltage of Q_1. Therefore, R_o is very large for small values of collector current.

The simplified small-signal model of the common-emitter amplifier with active load in Figure 6.29 is shown in Figure 6.30.

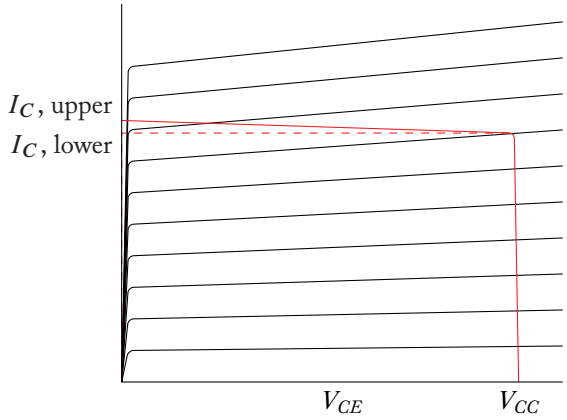


Figure 6.27: The characteristic curve of the active load device Q_1 superimposed on the output characteristic curves for Q_3.

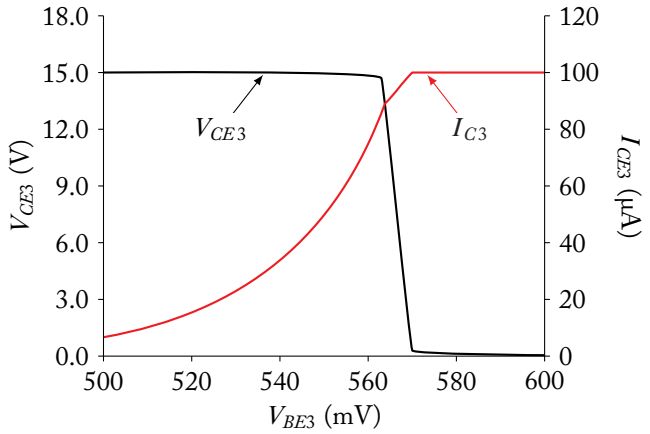


Figure 6.28: Q_3 collector current and voltage as a function of the input (base-emitter) voltage.

The small-signal output voltage of the amplifier is,

$$v_o = -h_{fe3}\, i_{b3} \left(h_{oe3}^{-1} \parallel R_O \right). \tag{6.129}$$

But, $i_{b3} = \frac{v_i}{h_{ie3}}$, so the gain of the amplifier is,

$$A_V = \frac{v_o}{v_i} = -\frac{h_{fe3}}{h_{ie3}} \left(h_{oe3}^{-1} \parallel R_O \right), \tag{6.130}$$

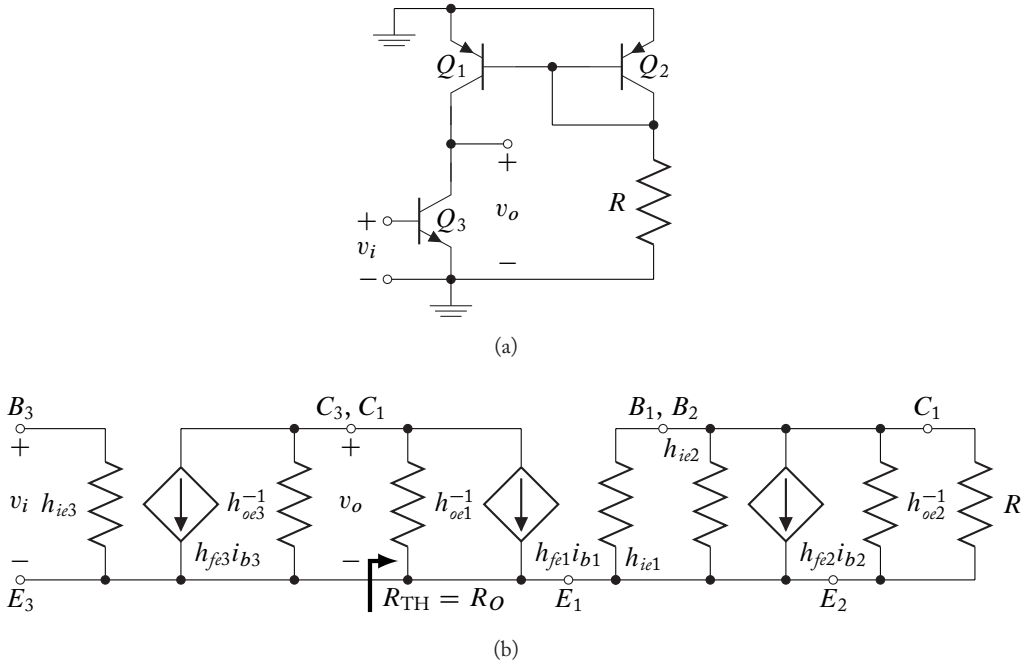


Figure 6.29: (a) AC and (b) Small-signal of the common-emitter amplifier with active load in Figure 6.26.

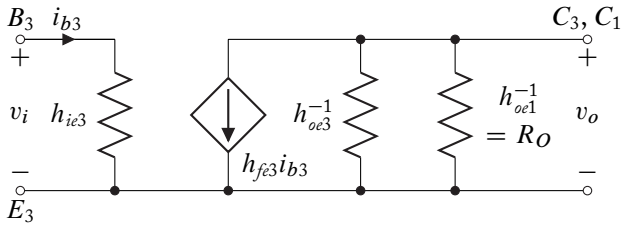


Figure 6.30: Simplified small-signal model of the common-emitter active load amplifier in Figure 6.26.

where from Equation (5.21),

$$h_{ie3} \approx (\beta_{F3} + 1)\frac{\eta V_t}{|I_{C3}|}. \tag{6.131}$$

Example 6.9

Design a common-emitter amplifier with an active load in the configuration shown in Figure 6.29. The lower current limit is required to be 100 μA. The following transistors are available for use:

2N2222 *npn*(IS=14.4E-15 BF=255 BR=6 VA=75)

2N2907 *pnp*(IS=650.6E-18 BF=232 BR=4 VA=116)

The power supply is +15 V.

Find the input resistance, small-signal gain, and other component values.

Solution #1

Design the common-emitter amplifier using the configuration in Figure 6.29. Find the resistor value R for the lower collector current limit of 100 μA. Rearranging Equation (6.128),

$$R = \frac{V_{CC} - V_{\gamma 1}}{\left(1 + \dfrac{2}{\beta_{FQ1}}\right) I_{C,lower}} = \frac{15 - 0.7}{\left(1 - \dfrac{2}{232}\right) 10^{-4}} = 143 \text{ k}\Omega \quad \text{(1\% standard value)}.$$

The upper limit of the collector current is found by first determining h_{oe1}^{-1}

$$R_O = \frac{1}{h_{oe1}} \approx \frac{V_{A1}}{I_{C,lower}} = \frac{116}{10^{-4}} = 1.16 \text{ M}\Omega.$$

The upper current limit is therefore approximately,

$$I_{C,upper} \approx I_{C,lower} + \frac{V_{CC} - V_{CE3(sat)}}{R_O} = 10^{-4} + \frac{15 - 0.2}{1.16 \times 10^6} = 113 \ \mu\text{A}.$$

For maximum output swing, select a bias point half-way between $I_{C,upper}$ and $I_{C,lower}$

$$I_{C,bias} = 106.5 \text{ mA}.$$

The base-emitter bias voltage for Q_3 is then,

$$V_{BE3(bias)} = \eta V_t \ln\left(\frac{I_{C,bias}}{I_{S3}} + 1\right) = (0.026) \ln\left(\frac{10^{-4}}{14.3 \times 10^{-15}} + 1\right) = 591 \text{ mV}$$

where $\eta = 1$.

The input resistance, R_i, is,

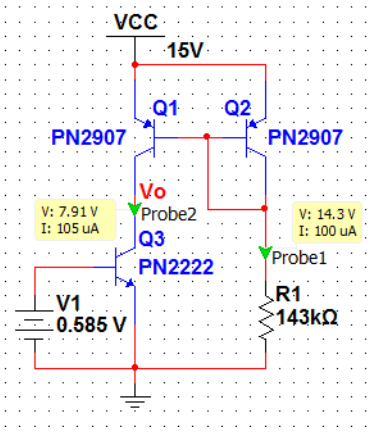
$$R_i = h_{ie3} \approx (\beta_{F3} + 1) \frac{\eta V_t}{|I_{C3}|} = (256) \frac{0.026}{106.5 \times 10^{-6}} = 62.5 \text{ k}\Omega.$$

The small-signal gain is then,

$$A_V = \frac{v_o}{v_i} = -\frac{h_{fe3}}{h_{ie3}} \left(h_{oe3}^{-1} \| R_O\right) = -\frac{255}{62.5 \text{ k}} (1.16M \| 1.16M) = -2.37 \text{ k}.$$

Solution #2. SPICE

The circuit in Figure 6.29 is simulated using SPICE using the value of R determined above with a reference current of 100 μA.



The result of the SPICE transfer function simulation are:

	Transfer Function Analysis	
1	Transfer function	−1.88605 k
2	vv1 #Input impedance	35.33296 k
3	Output impedance at V(V(vo),V(0))	466.12286 k

These results are in favorable agreement with the analytical results.

6.5.2 COMMON SOURCE AMPLIFIER WITH ACTIVE LOAD

An enhancement NMOSFET common source amplifier (M_1) with a PMOSFET current mirror active load is shown in Figure 6.31. FETs M_2 and M_3 form a current mirror where the reference current is determined by the resistor, R. For operation in the saturation region,

$$I_{REF} = I_{D3} = K_3(V_{GS3} - V_{T3})^2 \tag{6.132}$$

where

$$V_{GS3} = -V_{SG3} = -(V_{DD} - I_{REF}R)\,. \tag{6.133}$$

By substituting Equation (6.133) into (6.132), the reference current is found as a function of R.

The transistor M_1 is in cutoff when $V_{GS} < V_T$. Under this condition, no current flows through M_2 and, because it is a current mirror, M_3. As V_{GS} increases above V_T, M_1 enters saturation and forces M_2 into the ohmic region and lowers V_O. Further increase in the input voltage

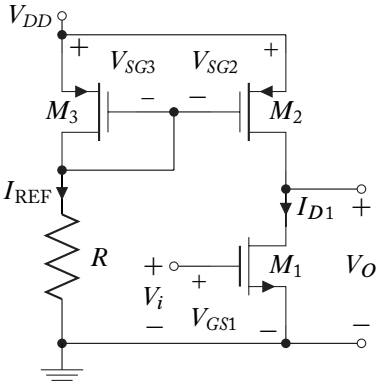


Figure 6.31: Common source amplifier with active load.

forces M_2 into saturation decreasing the output voltage. Finally, M_1 enters the ohmic region while M_2 and M_3 remain in the saturation region.

The transfer function of the active load common source amplifier of Figure 6.31 is shown in Figure 6.32.

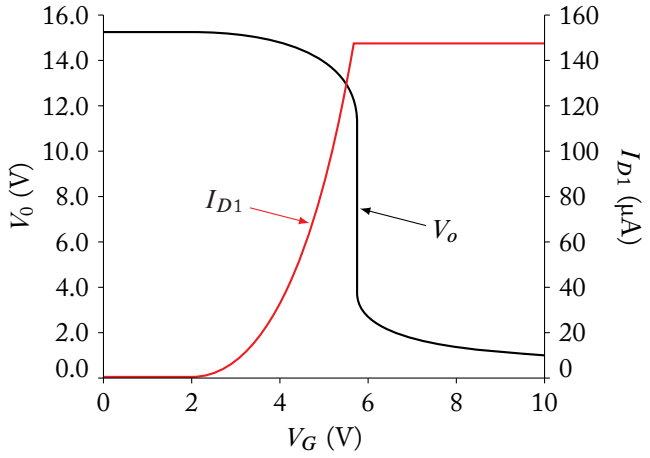


Figure 6.32: Transfer characteristic of the active-load common-source amplifier in Figure 6.31.

The small-signal model of the amplifier is used to determine the gain of the amplifier. The AC model of Figure 6.25 is shown in Figure 6.27.
From the AC model in Figure 6.33, the small-signal model can be derived, and is shown in Figure 6.34. The load resistor consists only of the drain resistance of M_2.

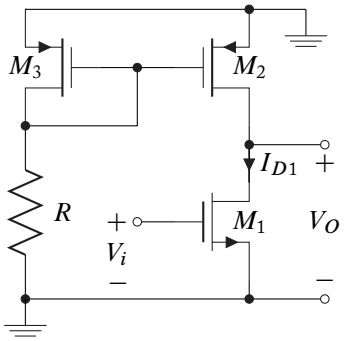


Figure 6.33: AC model of the common source amplifier with active load of Figure 6.31.

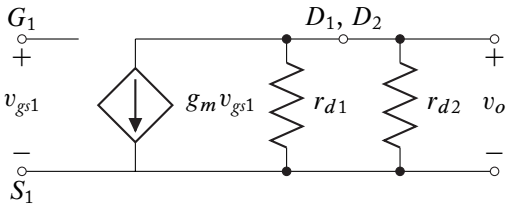


Figure 6.34: Small-signal model of the common source amplifier with an active load.

The drain resistance is found by applying Equation (5.144),

$$r_d = \frac{|V_A|}{|I_D|}. \tag{6.134}$$

The small-signal transconductance is defined in Equation (5.132) as,

$$g_m = 2K\left(V_{GS} - V_T\right) = 2\sqrt{I_D K}. \tag{6.135}$$

The gain of the amplifier is,

$$A_V = g_{m1}\left(r_{d1} // r_{d2}\right). \tag{6.136}$$

6.5.3 EMITTER-COUPLED DIFFERENTIAL AMPLIFIER WITH ACTIVE LOAD

An emitter-coupled differential amplifier with an active load current mirror is shown in Figure 6.35. It is assumed that Q_3 and Q_4, and Q_1 and Q_2 are matched pairs. In this circuit, the collector current is controlled by the Q_1 side of the emitter coupled pair. It is also a single-ended output amplifier, which eliminates the common mode problem and has higher CMRR than a single output differential amplifier with resistive loads.

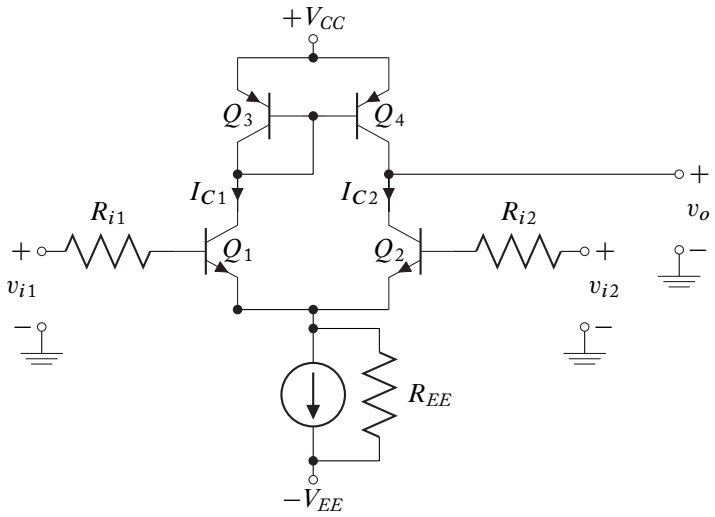


Figure 6.35: Emitter-coupled single-ended output differential amplifier with active load current mirror.

The AC model of the emitter-coupled single-ended differential amplifier with an active load of Figure 6.35 is shown in Figure 6.36. The gain for the circuit in Figure 6.36 is performed by using a single input at v_{i1} and grounding v_{i2}.

Since Q_3 and Q_4 form a current mirror, the collector current $i_{c1} = h_{fe1} i_{b1}$ through transistor Q_1 is equal to the collector current through Q_2. Since the output resistance of the common-base transistor, Q_2, is much greater than that of the common-emitter transistor, Q_4, the output voltage is then,

$$v_o = \frac{h_{fe1} i_{b1}}{h_{oe4}}. \tag{6.137}$$

The emitter resistance of Q_1 must be found to determine the base current i_{b1}. The emitter of Q_1 is connected to R_{EE} and the emitter of Q_2. Q_2 appears as a common-base configuration with an input resistance,

$$R_{E2} \approx \left(\frac{h_{ie2} + R_{i2}}{h_{fe2} + 1} \right) // R_{EE} \approx \frac{h_{ie2} + R_{i2}}{h_{fe2} + 1}, \tag{6.138}$$

for a large h_{oe4}^{-1} and R_{EE}.

The base current for Q_1 is found by using Equation (6.138),

$$i_{b1} = \frac{v_{i1}}{(R_{i1} + h_{ie1}) + \left[(h_{fe1} + 1) \left(\frac{h_{ie2} + R_{i2}}{h_{fe2} + 1} \right) \right]} \tag{6.139}$$

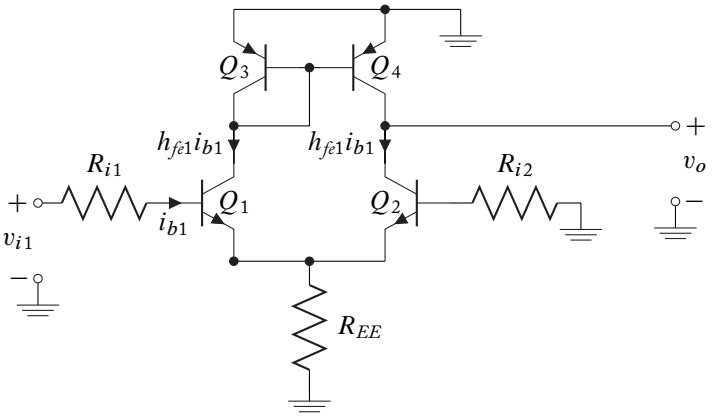


Figure 6.36: AC model of the emitter coupled differential amplifier in Figure 6.35.

By substituting Equation (6.139) into (6.137), the output voltage is,

$$v_o = \frac{h_{fe1}v_{i1}}{h_{oe4}(2R_{i1} + 2h_{ie1})} = \frac{h_{fe1}v_{i1}}{2h_{oe4}(R_{i1} + h_{ie1})}. \tag{6.140}$$

Therefore, the gain of the amplifier is,

$$A_v = \frac{v_o}{v_{i1}} = \frac{h_{fe1}}{2h_{oe4}(R_{i1} + h_{ie1})} \tag{6.141}$$

This result is exactly one-half of that predicted by Equation (6.65) where the load resistance is given by:

$$R_c = \frac{1}{h_{oe4}}.$$

The factor of two is the result of the single-ended rather than differential output.

6.6 CONCLUDING REMARKS

The range of transistor amplifiers available for use was expanded in this chapter to include the use of multiple transistor applications. This extension to allows the designer to create amplifiers that have a combination of amplification, input resistance, and output resistance that is not within the capabilities of single transistor amplifiers.

Cascaded-stage designs, consisting of several simple stages in series, are the dominant form of multiple transistor amplifiers. Closely related to cascaded-stage designs are the Darlington and similar grouped-transistor amplification stages.

Other common multiple transistor amplification stages are based on differential inputs rather than inputs solely referenced to a common terminal. Emitter coupled and source coupled

transistor pairs form the basis for differential amplifiers. Among the many needs for differential inputs are many OpAmp applications.

While the addition of additional amplification stages complicates the process, the modeling and analysis techniques for multiple transistor amplifiers follow the same basic procedure that has been previously described:

1. Determine the quiescent (DC) conditions—verify all transistors are in the proper operating region
2. Determine the small-signal parameters for each transistor from the quiescent conditions
3. Create an AC equivalent circuit
4. Determine the AC performance for the circuit
5. Add the results of the DC and AC analysis to obtain total circuit performance.

Although each step of the procedure may be more complicated, simple steps taken together provide the desired results.

Integrated circuit amplifier designs are an area where the use of multiple transistors prevails. In discrete applications resistors are cost effective and reliable; in IC applications they create a multitude of design obstacles. The use of multiple-transistor current sources as amplifier bias networks solves many of the problems. Current sources can also provide high resistance active loads for many of the single and multiple transistor amplifier types. Active loads provide high gain without the use of large resistors or high-voltage sources.

While the interconnection of many transistors in simple amplifiers can satisfy many design goals, it does not always provide the optimum design. The sensitivity of these designs to transistor parameter variation is, on occasion, a concern. High power applications also put constraints on amplifier designs. These design concerns and several solutions are explored in Chapters 7 and 8.

Summary Design Example

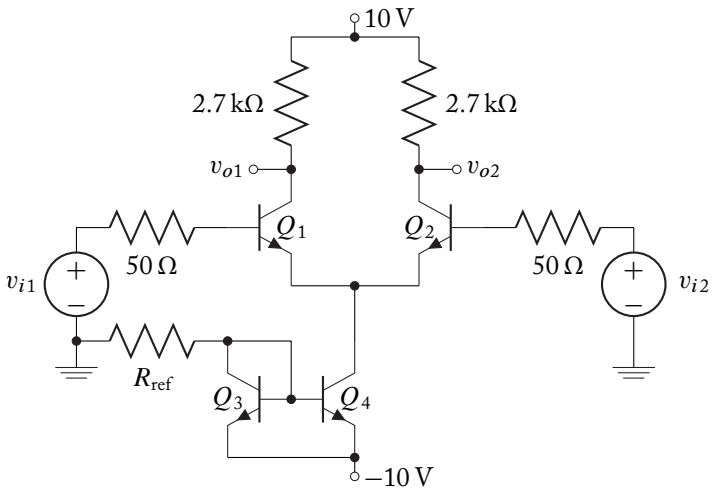
A particular electronic application requires the amplification of the difference of two voltages by a factor of 200 ± 20. Each input source has an output resistance of $50\,\Omega$. The output of the amplifier must also be differential with each output having an output resistance of $2.7\,\text{k}\Omega$. Available voltages sources are at ground potential and 10 V. It is expected that this design may eventually realized in a bipolar IC application where the individual BJTs are described by:

$$\beta_F = 200 \qquad V_A = 160.$$

Solution:

The design requirements suggest a emitter-coupled differential amplifier. The possibility of eventual IC realization implies that the differential pair should be biased with a BJT current

source. The basic topology of the circuit is therefore as shown at the right (the load and source resistors are specified above):



The differential gain of this circuit is given by:

$$A_{VD} = \frac{-h_{fe}R_c}{h_{ie} + 1/2\{R_{i1} + R_{i2}\}}$$

This gain requirement restricts the differential pair BJT parameter, h_{ie}:

$$h_{ie} = \frac{h_{fe}R_c}{A_{VD}} - 1/2\{R_{i1} + R_{i2}\} = 2650\,\Omega.$$

Such a value can only be achieved with a specific collector current in each of the differential pair BJTs:

$$h_{ie} = (\beta_F + 1)\frac{\eta V_t}{I_C} \quad \Rightarrow \quad I_C = 1.972\text{ mA}.$$

The bias current provided by the current source must be the sum of the differential pair emitter currents:

$$I_{bias} = 2\left(\frac{\beta_F + 1}{\beta_F}\right) I_C = 3.964\text{ mA}.$$

This bias current can be directly related to the collector currents of the two current source BJTs:

$$I_{bias} \approx I_{C4} + (10 - V_\gamma)h_{oe4} = I_{C4}\left(1 + \frac{9.3}{V_A}\right) \quad \Rightarrow \quad I_{C4} = 3.746\text{ mA}$$

The current source bias resistor value can then be determined:

$$R_{REF} = \frac{10 - V_\gamma}{3.746\left(1 + \frac{2}{200}\right)} = 2.458\text{k}\Omega \approx 2.46\,\text{k}\Omega.$$

SPICE simulation shows the differential gain of this amplifier to be ≈ 193, which is within specifications.

6.7 PROBLEMS

6.1. The amplifier shown uses identical transistors with the following characteristics:

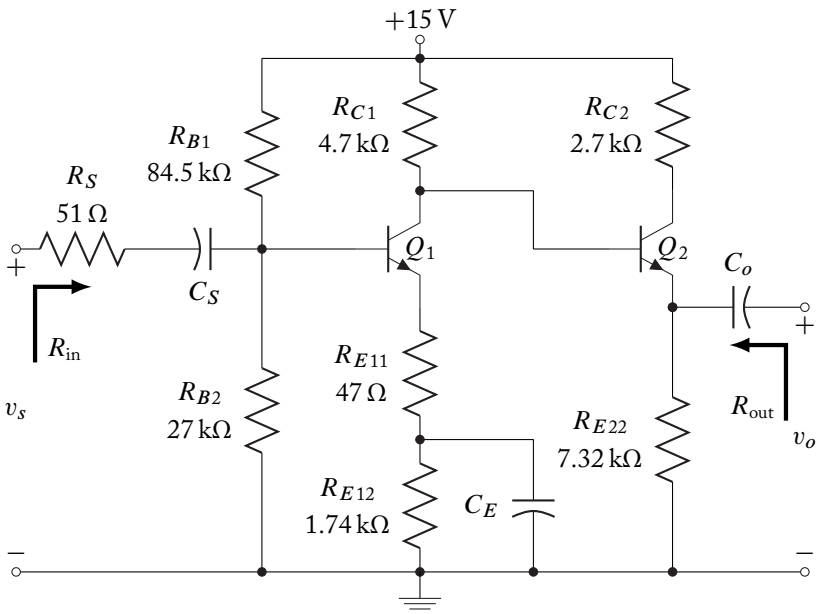
$$\beta_{F1} = 220,$$
$$\beta_{F2} = 180,$$
$$V_{A1} = V_{A2} = 200\,\text{V}.$$

(a) Determine the quiescent currents and voltages of each transistor.

(b) Find the overall voltage gain, A_{vs}.

(c) Find the input resistance, R_{in}.

(d) Find the output resistance, R_{out}.



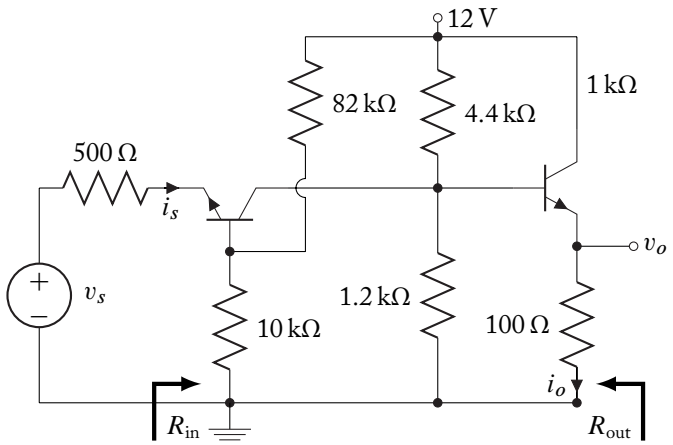
6.2. Determine the voltage gain,

$$A_V = \frac{v_o}{v_s},$$

current gain,

$$A_I = \frac{i_o}{i_s},$$

input resistance, R_{in}, and output resistance, R_{out}, for the given two-stage cascade amplifier. The Silicon BJTs are identical and are described by $\beta_F = 150$.



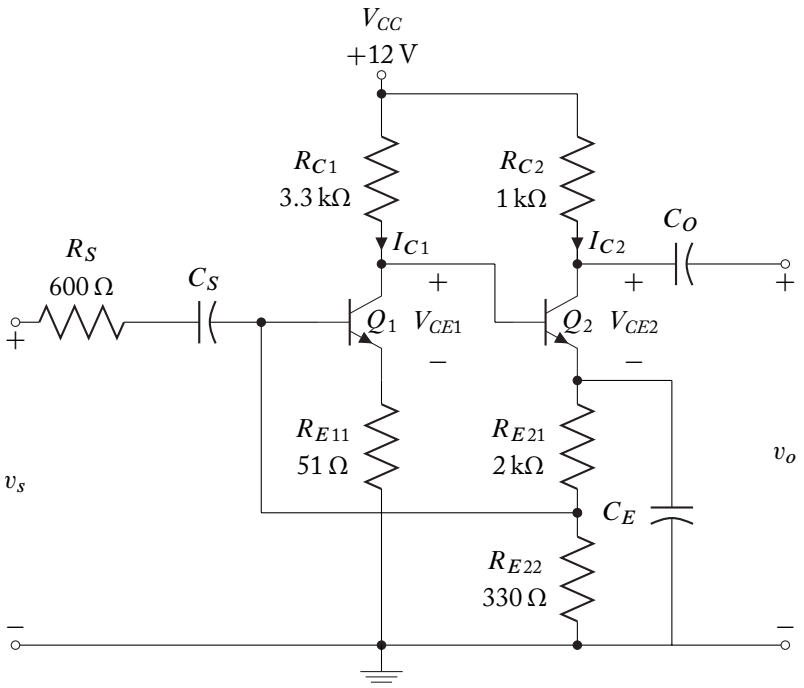
6.3. The amplifier shown uses identical transistors with the following characteristics:

$$\beta_F = 180$$
and
$$V_A = 200\,\text{V}.$$

(a) Find the quiescent point of the transistors

(b) Find the midband voltage gain of the amplifier.

(c) Confirm the results using SPICE.



6.4. It is usually not a good design choice to cascade two simple common-collector amplifier stages. Investigate this cascade by performing the following design:

(a) Using a Silicon BJT with $\beta_F = 150$, design a simple one transistor, common-collector amplifier to meet the following design goals:

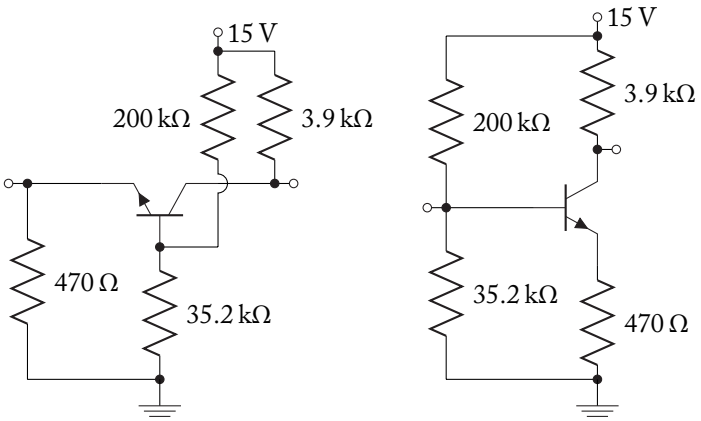
Emitter Resistor,	$R_e = 1\,\text{k}\Omega$	
Power Supply,	$V_{CC} = 10\,\text{V}$	
Q-point	$V_{CEQ} = 5\,\text{V}$	
Stage Input Resistance,	$R_{in} = 20\,\text{k}\Omega$	(includes bias resistors).

(b) Determine the voltage gain, current gain, and output resistance of this simple stage

(c) Capacitively cascade two stages of the design from part a—compare performance characteristics (including input resistance) of this two-stage amplifier with the single-stage amplifier of part b). Comment on results.

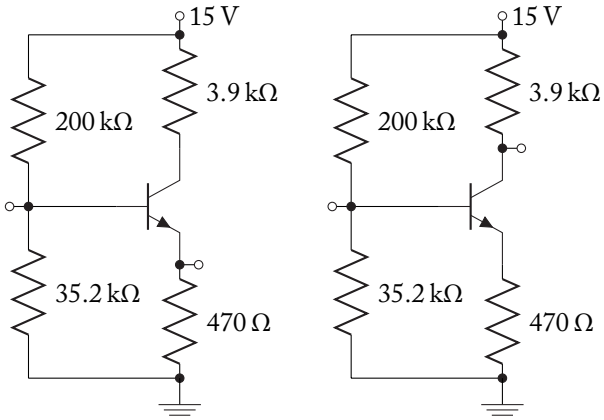
6.5. In most multistage amplifier designs, common-base amplifier stages are best used as input stages to an amplifier cascade: they have little value when used as intermediate or final stages. Investigate this simple design principle by comparing the voltage and current gain of two-stage, capacitively-coupled cascades consisting of the two given amplifiers in the two configurations: CB-CE and CE-CB.

Assume Silicon BJTs with $\beta_F = 100$.



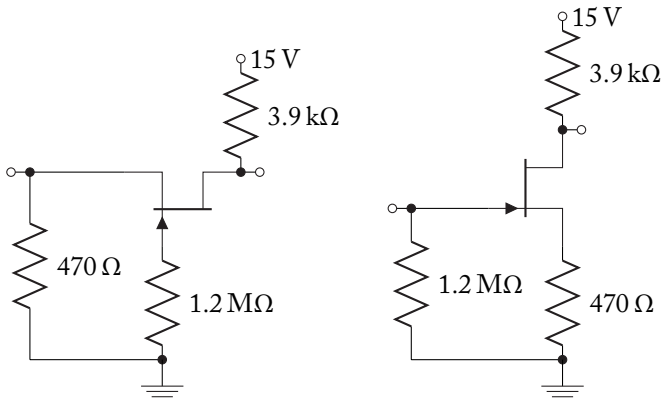
6.6. In most multistage amplifier designs, common-collector amplifier stages are best used as output stages to an amplifier cascade: they have little value when used as input or intermediate stages. Investigate this simple design principle by comparing the voltage and current gain of two-stage, capacitively-coupled cascades consisting of the two given amplifiers in the two configurations: CC-CE and CE-CC.

Assume Silicon BJTs with $\beta_F = 100$.



6.7. In most multistage amplifier designs, common-gate amplifier stages are best used as input stages to an amplifier cascade: they have little value when used as intermediate or final stages. Investigate this simple design principle by comparing the voltage and current gain of two-stage, capacitively-coupled cascades consisting of the two given amplifiers in the two configurations: CG-CS and CS-CG.

Assume FET parameters: $I_{DSS} = 4\,\text{mA}$, $V_{PO} = -2\,\text{V}$ and $V_A = 150\,\text{V}$.



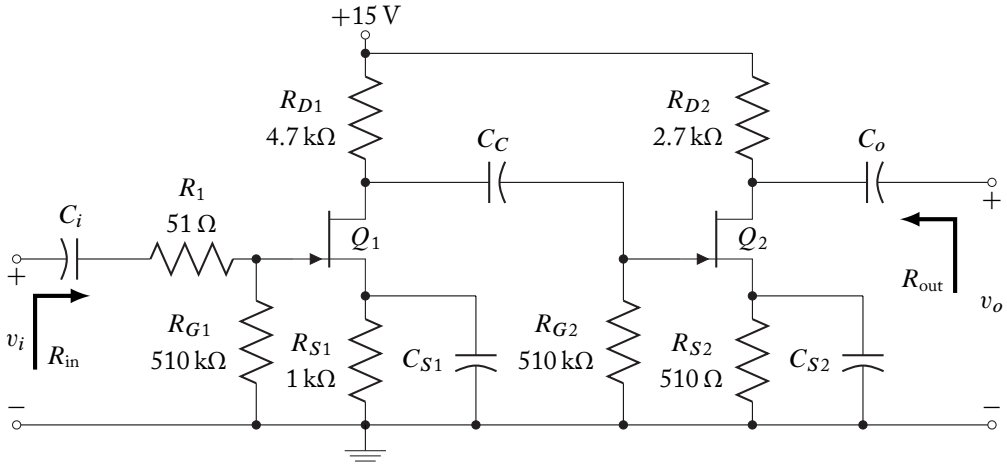
6.8. The amplifier shown uses identical transistors with the following characteristics:

$$I_{DSS} = 10\,\text{mA},\ V_{PO} = -2\,\text{V}, \quad \text{and} \quad V_A = 100\,\text{V}.$$

(a) Find the overall voltage gain A_{vs}.

(b) Find the input resistance R_{in}.

(c) Find the output resistance R_{out}.



6.9. For the circuit shown, the transistor parameters are:

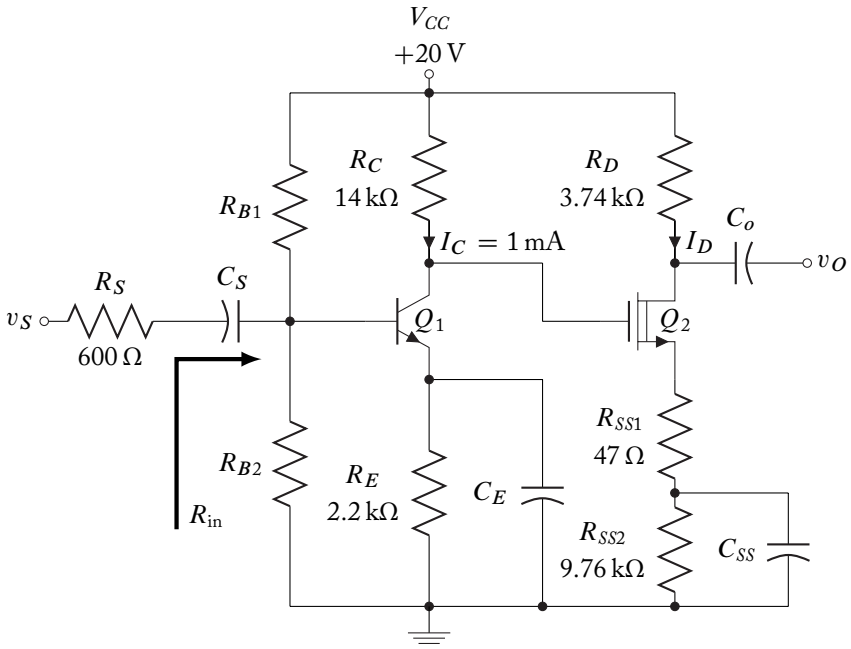
$$Q_1: \quad \beta_F = 200,\ V_\gamma = 0.7\,\text{V},\ V_A = 250\,\text{V}$$
$$Q_2: \quad I_{DSS} = 10\,\text{mA},\ V_{PO} = -5\,\text{V},\ V_A = 250\,\text{V}.$$

(a) Find R_{B1} and R_{B2} for $I_C = 1\,\text{mA}$. Use the "rule of thumb" relationship between R_E and R_B for stable operation (1% change in I_C for 10% change in β_F).

(b) Find the quiescent condition of the two transistors.

(c) Find the voltage gain of the amplifier

(d) Find the input resistance, R_{in}, of the amplifier.



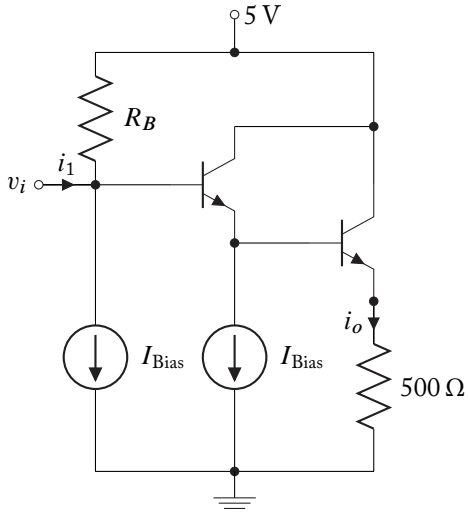
6.10. For the given Darlington circuit:

(a) Determine the values of the two identical current sources, I_{Bias}, and the bias resistor, R_B, so that the quiescent BJT collector currents are the same value and the quiescent output voltage is 2.5 V. The Silicon BJTs are identical with

$$\beta_F = 200,\ V_A = 350\,\text{V}.$$

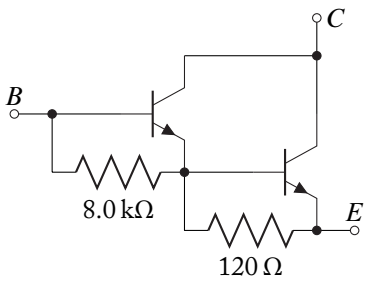
(b) Determine the small-signal h-parameters for the composite Darlington transistor.

(c) Find the current gain of the circuit: $A_I = i_o/i_s$.



6.11. Many Darlington Silicon power transistor pairs provide built-in base-emitter shunt resistors as an aid to biasing. One such Darlington pair is the 2N6387 for which a typical circuit diagram is shown at the right. For DC analysis purposes these resistors act as current sources of value:

$$I_{Bias} = \frac{V_\gamma}{R_{\text{shunt}}}$$



In AC analysis the resistors slightly decrease the effective value of the two dominant h-parameters, h_{ie} and h_{fe}, in each BJT. For this Darlington pair assume each individual BJT in the typical circuit diagram is described by $\beta_F = 60$.

(a) Design a common-collector amplifier using the following parts to achieve a quiescent collector current for the Darlington pair of 3 A.

DC power supply,	$V_{CC} = 48$ V
Load resistor	$R_L = 8\,\Omega$ (at the emitter)
Single bias resistor	$R_B =$ any value (use only 1 resistor)

(b) Determine the effective small-signal h-parameters of each of the Darlington transistors (find the h-parameters for each BJT with its B-E junction shunted) and the Darlington pair as a whole.

(c) Determine the performance characteristics of the amplifier, that is find A_V, A_I, and R_{in}.

6.12. The transistors in the circuit at the right have parameters:

$$I_{DSS} = 2\,\text{mA} \quad V_{PO} = -2\,\text{V} \quad V_A = 100\,\text{V},$$

and

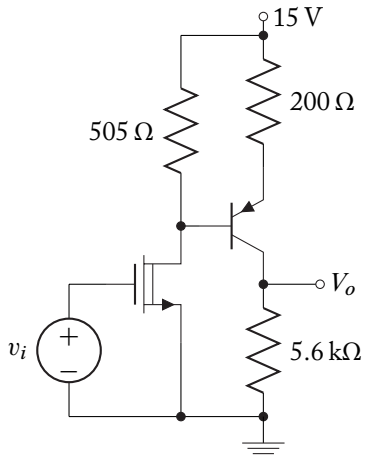
$$\beta_F = 150 \quad V_A = 200\,\text{V}.$$

The quiescent conditions have been found to be:

$$|I_{DQ}| = 2\,\text{mA} \qquad V_{DSQ} = 14\,\text{V}$$
$$|I_{CQ}| = 1.515\,\text{mA} \quad V_{CEQ} = 6.21\,\text{V}$$

(a) Determine the small-signal parameters for the two transistors.

(b) Determine the voltage gain of the circuit.



6.13. For the amplifier shown, the transistor characteristics are:

JFET: $I_{DSS} = 8\,\text{mA}$

$$V_{PO} = -5\,\text{V} \qquad V_A = 100\,\text{V}.$$

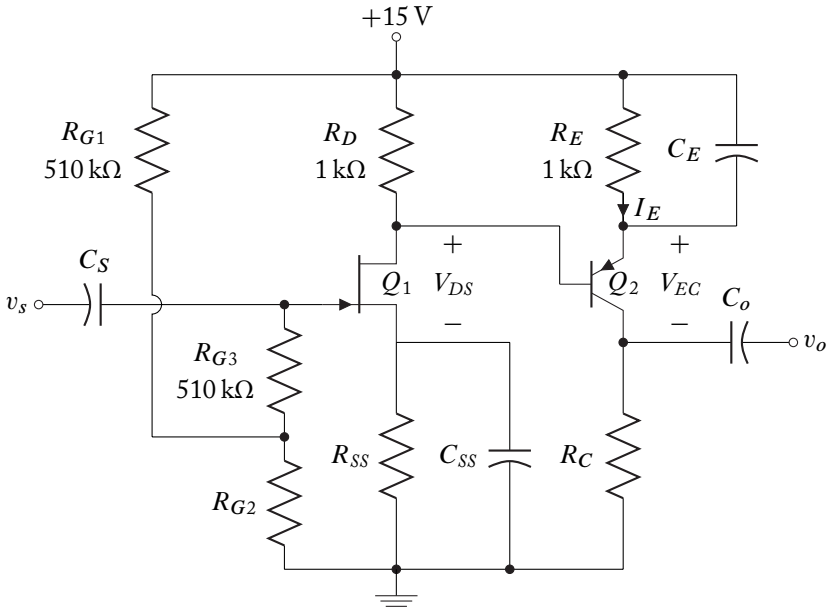
BJT: $\beta_F = 200$

$$V_A = 100\,\text{V}.$$

(a) Complete the design of the amplifier so that $I_E = 3\,\text{mA}$, and $V_{DS} = V_{EC} = 5\,\text{V}$. Find the quiescent point of all of the transistors

(b) Find the midband voltage gain of the amplifier.

(c) Confirm the results using SPICE.



6.14. Complete the design of the amplifier shown.

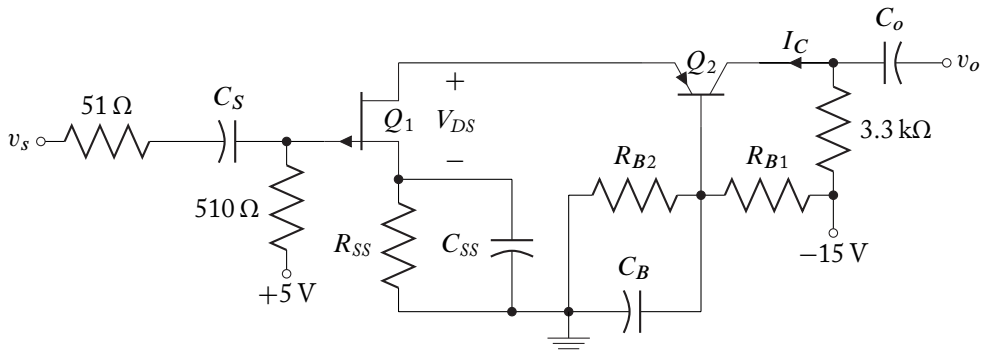
The transistor parameters are:

$$JFET: I_{DSS} = -8\,\text{mA},\ V_{PO} = 3.5\,\text{V},\ V_A = 100\,\text{V}$$
$$BJT: \beta_F = 120\ V_A = 150\,\text{V}.$$

(a) Find R_{SS}, R_{B1}, and R_{B2} so that $I_C = -1\,\text{mA}$ and $V_{DS} = -3.9\,\text{V}$. Determine the quiescent points of the transistors.

(b) Determine the midband voltage gain of the amplifier

(c) Confirm the results using SPICE.



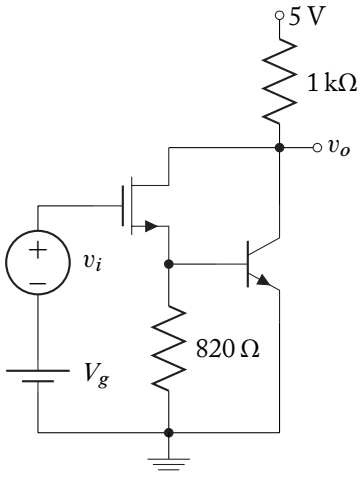
6.15. For the BiFET Darlington configuration shown, the bias voltage V_g is adjusted so that the quiescent output voltage is 2.5 V. The transistor parameters are as follows:

$$\beta_F = 200 \qquad V_A = 150\,\text{V}$$
$$K = 1\,\text{mA/V}^2 \qquad V_T = 2\,\text{V}.$$

(a) Determine V_g.

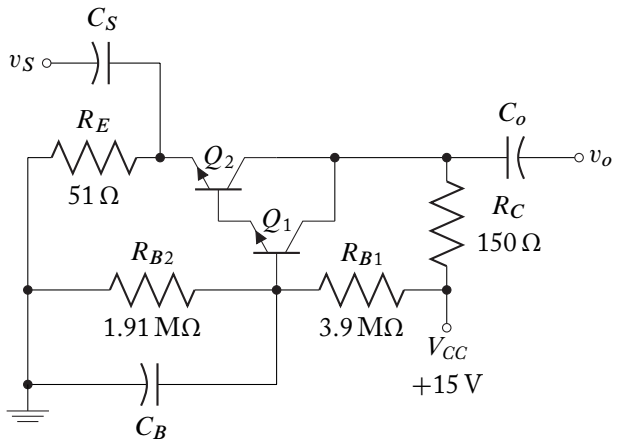
(b) Find the voltage gain of the circuit:

$$A_V = \frac{v_o}{v_i}.$$



6.16. Determine the quiescent currents and voltages, and the midband voltage gain of the Darlington common-base amplifier shown below. Identical transistors are used with parameters:

$$\beta_F = 180,\ V_A = 200\,\text{V}.$$



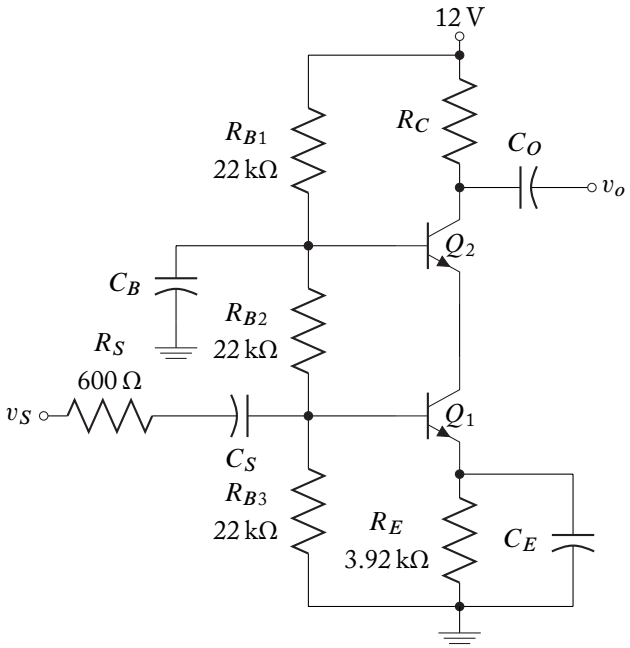
6.17. For the circuit shown, the transistors parameters are:

$$\beta_F = 180,\ V_\gamma = 0.7\,\text{V},\ V_A = 250\,\text{V}.$$

(a) Complete the design by finding R_C.

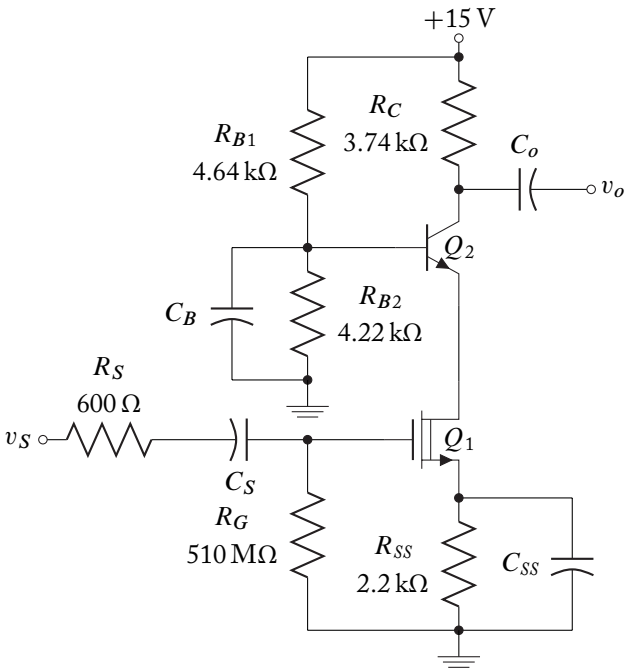
(b) Find the quiescent condition of the two transistors.

(c) Find the voltage gain of the amplifier



6.18. Determine the quiescent currents and voltages, and the midband voltage gain of the FET/Bipolar cascode amplifier shown below. The transistor parameters are:

$$\begin{aligned} Q_1: \quad & V_{PO} = -4\,\text{V}, \\ & I_{DSS} = 5\,\text{mA}, \\ & V_A = 200\,\text{V}. \\ Q_2: \quad & \beta_F = 220, \\ & V_A = 250\,\text{V}. \end{aligned}$$

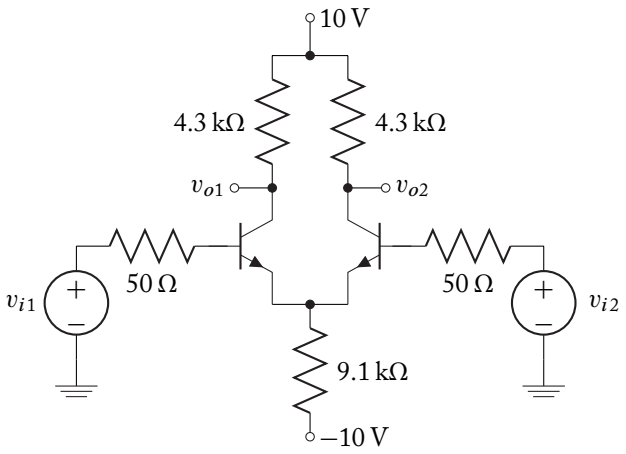


6.19. The differential amplifier shown utilizes a simple emitter resistor to establish quiescent conditions. Assume identical BJTs with

$$\beta_F = 120.$$

(a) Determine the differential-mode gain.

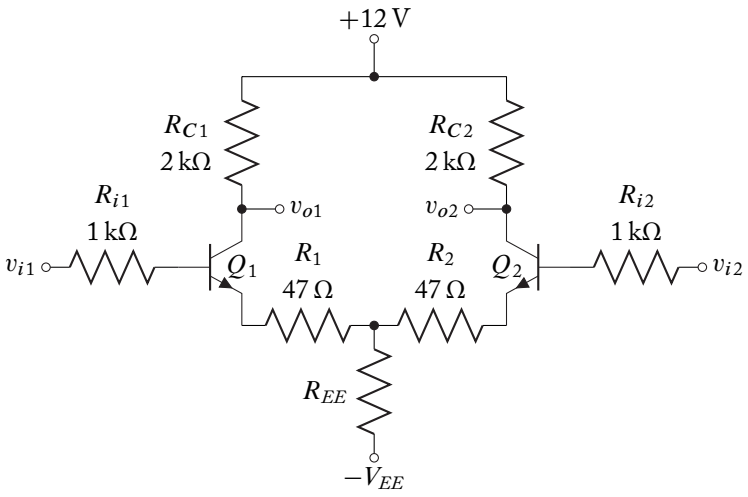
(b) Determine the common-mode rejection ratio (CMRR).



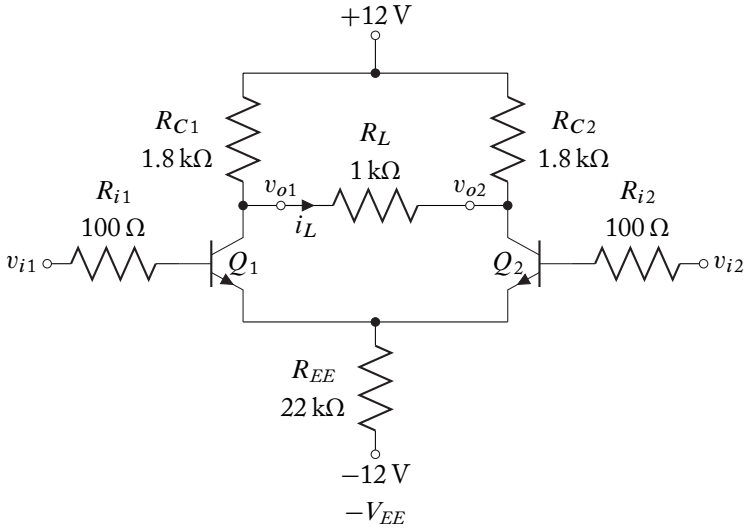
6.20. Complete the design of the differential amplifier shown below so that the CMRR = 43 dB. Assume identical transistors with $\beta_F = 120$.

(a) Find R_{EE} and V_{EE}.

(b) Confirm the results using SPICE.



6.21. For the differential amplifier shown, find i_L in terms of the common- and differential-mode input signals. Assume identical transistors with $\beta_F = 120$.



6.22. The transistors in the differential amplifier shown below are identical and have the following characteristics:

$$I_{DSS} = 10\,\text{ma},\ V_{PO} = -4.5\,\text{V},$$
$$V_A = 100\,\text{V}.$$

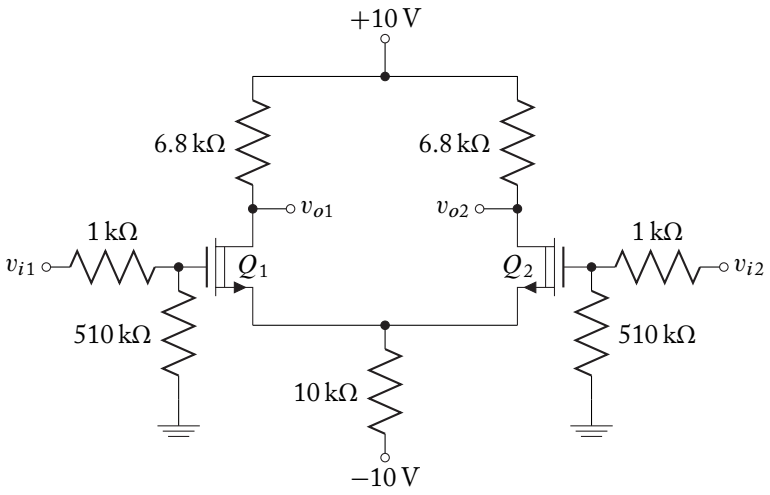
(a) Find the CMRR

(b) Determine the output voltage:

$$v_{02} - v_{01}.$$

(c) The output resistance looking into the drain of Q_2.

(d) Use SPICE to confirm the output voltage found in part (b) and the output resistance found in part (c).



6.23. Design a 100 μA Widlar current source utilizing two identical Silicon BJTs with parameters:

$$\beta_F = 150 \qquad V_A = 250\,\text{V},$$

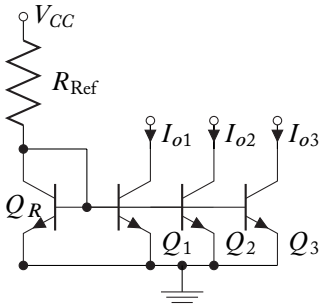
two resistors, and a 10 V battery. In order to extend battery life, total power consumption must be less than 10 mW.

6.24. It is often necessary in integrated circuit applications to design a current source with multiple outputs. The general topology of a simple current mirror with three outputs is shown.

(a) Determine the magnitude of output currents as a function of the circuit parameters.

(b) Generalize the results of part a for circuits with n outputs.

(c) Design a four-output current source using Silicon BJTs with $\beta_F = 120$ and a voltage source of 10 VDC to have identical output currents of 300 μA.



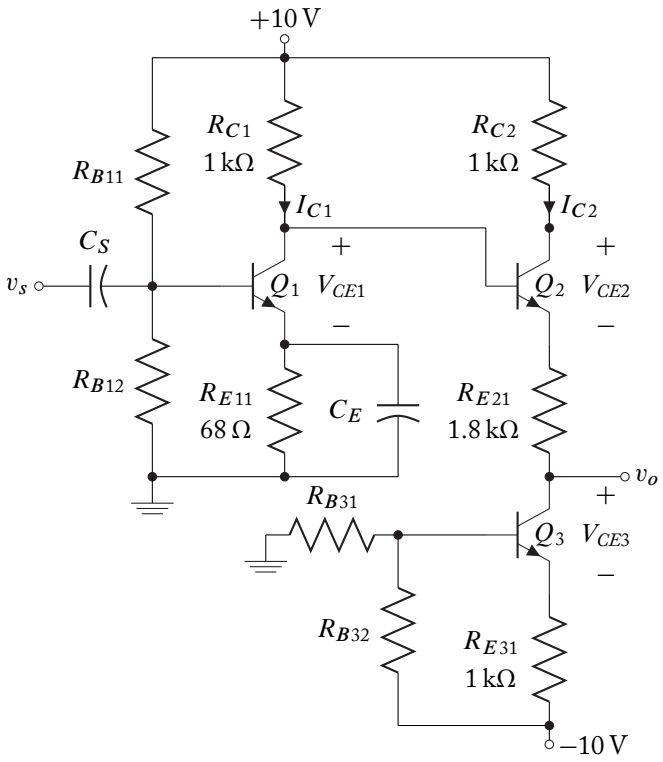
6.25. Complete the design of the amplifier shown so that the quiescent value of the output voltage, v_o, has value $+1$ V. The transistors are identical and have the following characteristics:

$$\beta_F = 200 \qquad \text{and} \qquad V_A = 200\,\text{V}.$$

(a) Find the quiescent point of the transistors

(b) Find the midband voltage gain of the amplifier.

(c) Confirm the results using SPICE.



6.26. Design a simple enhancement-mode NMOSFET current mirror for a load current of 50 μA. Use identical transistors with the parameters $K = 0.5\,\text{mA/V}^2$ and $V_T = 2$ V. Confirm the analytical design using SPICE.

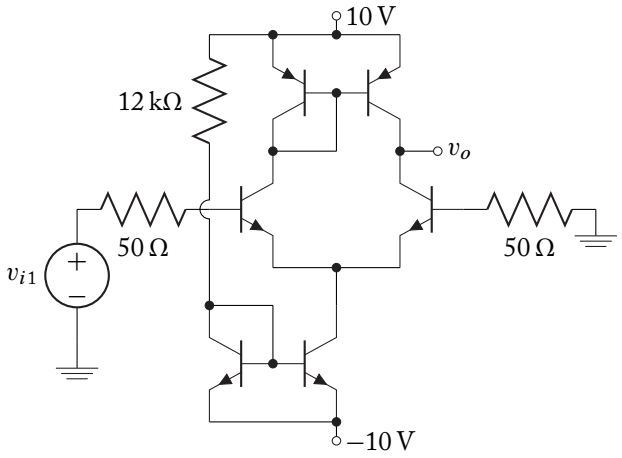
6.27. Design a simple depletion-mode NMOSFET current mirror for a load current of 30 μA. Use identical transistors with the parameters $I_{DSS} = 10$ mA and $V_{PO} = -4$ V. Confirm the analytical design using SPICE.

6.28. The emitter-coupled amplifier shown utilizes a current source to establish quiescent conditions and another to provide a high resistance load. Assume BJTs with

$$\beta_F = 120,\ V_A = 250.$$

(a) Determine the voltage gain and the input resistance of the circuit.

(b) Verify analytic results using SPICE.



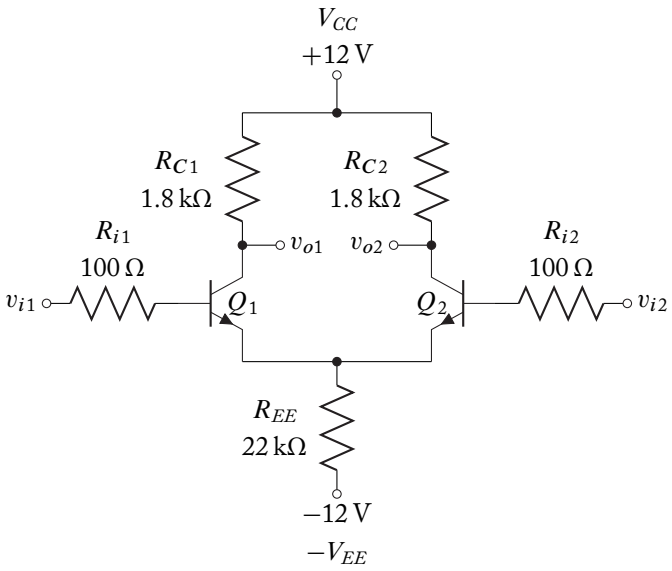
6.29. The differential amplifier shown uses identical BJTs. The BJT parameters are:

$$\beta_F = 200,\ V_A = 250\,\text{V}.$$

(a) Determine the midband differential-mode and common-mode voltage gains.

(b) Design a Wilson current mirror using three identical BJTs to replace R_{EE} using the ± 12 V power rails. The BJTs for the current mirror are identical to the BJTs for the differential amplifier.

(c) What is the midband differential-mode and common-mode voltage gains of the differential amplifier biased by the Wilson current mirror?



6.30. Using appropriate analysis and complete explanations:

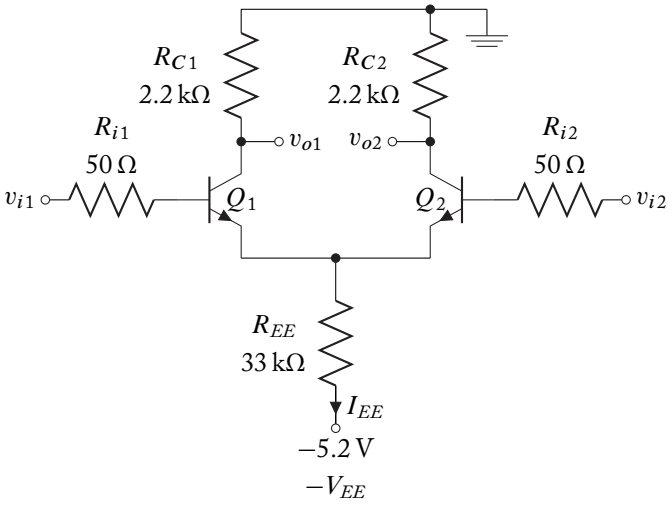
(a) Find the quiescent condition for the differential amplifier shown. The transistors are identical with parameters: $\beta_F = 200$, $V_\gamma = 0.7\,\text{V}$, $V_A = 250\,\text{V}$.

(b) How large can R_{C1} and R_{C2} become in this design if the bias current I_{EE} is to remain constant at the value found in part (a) and still remain a viable amplifier?

(c) Design a simple two transistor current mirror to replace R_{EE}.

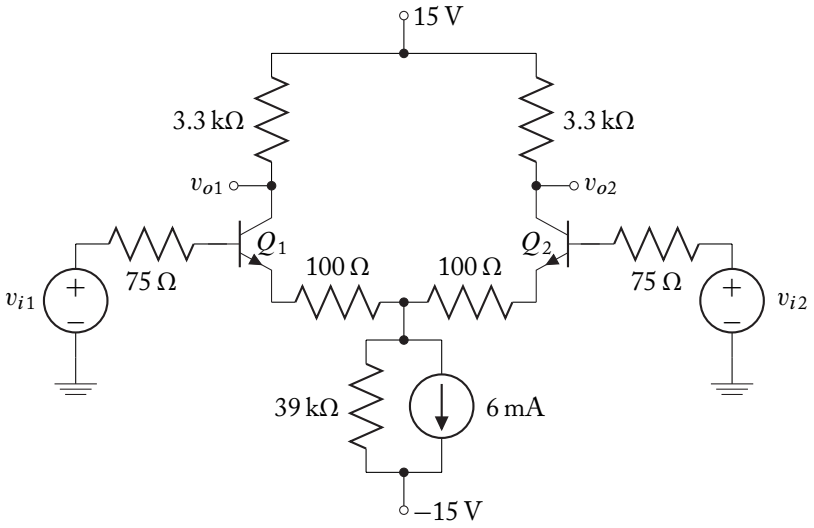
(d) What is the impact on the amplifier CMRR if R_{EE} is replaced by a simple current mirror in the differential amplifier design?

(e) What are the design advantages to replacing R_{C1} and R_{C2} with an active load designed from a simple two transistor *pnp* current mirror?



6.31. In order to boost the input resistance of a differential amplifier, resistors are often added between the emitters of the emitter-coupled BJT pair. For the circuit shown calculate the differential voltage gain, input resistance, and the CMRR. Compare appropriate results with a circuit without these emitter resistors (Examples 6.4 and 6.5).

Assume identical BJTs with $\beta_F = 120$.



6.32. The Darlington differential amplifier, shown is designed using identical transistors with

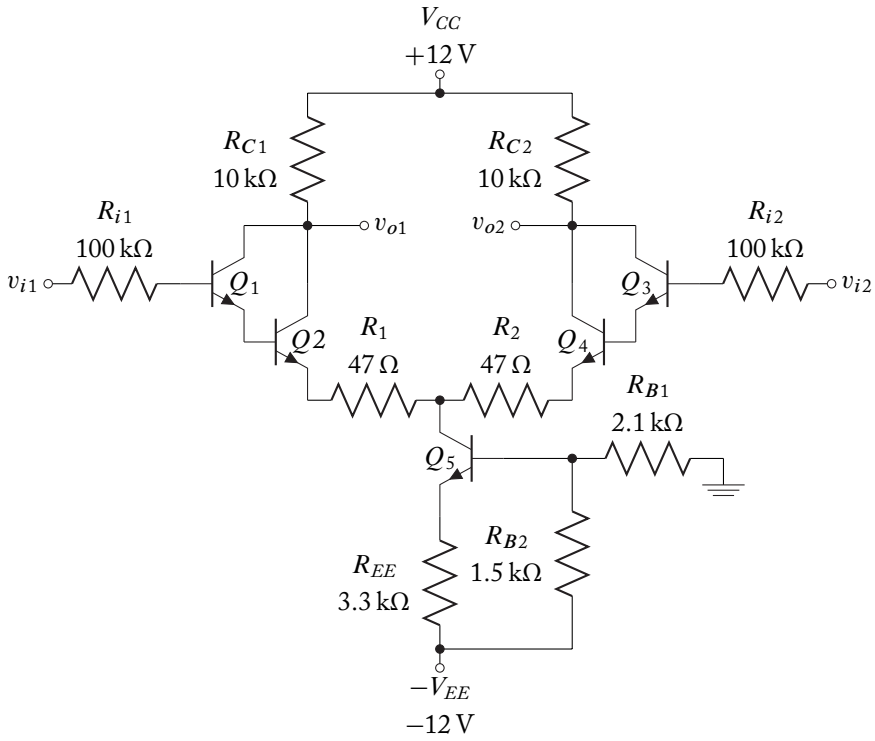
$$\beta_F = 120 \quad \text{and} \quad V_A = 200\,\text{V}.$$

(a) Determine the quiescent operating conditions.

(b) Find the CMRR

(c) Determine the output voltage:

$$v_{02} - v_{01}.$$



6.33. Design a common-emitter amplifier with an active load. The lower current limit specification is 50 μA. The following transistors are available:

$$2N2222A\ npn\ (\text{IS} = 14.4\text{f BF} = 255\ \text{VA} = 175)$$
$$2N2907\ \ pnp\ (\text{IS} = 650\text{E-18 BF} = 232\ \text{VA} = 116).$$

The power supply is +24 V.

(a) Find the input resistance of the amplifier.

(b) Find the small-signal midband gain.

(c) Confirm the analytical results with SPICE.

6.34. Design a common-source amplifier with an active load using enhancement NMOSFETs so that the gain of the amplifier is -25 ± 5. The following transistors are available:

.model PMOSFET PMOS(VTO = 2 KP = 20E-6 LAMBDA = 0.01)
.model NMOSFET NMOS(VTO = 2 KP = 20E-6 LAMBDA = 0.01)

Confirm the analytical results with SPICE.

6.35. A differential *npn* BJT amplifier is biased by a 150 μA emitter bias source. The collector load resistors are mismatched by 5%. Find the offset voltage required at the input so that the differential output voltage is zero.

6.36. A differential amplifier is design with two *npn* BJT transistors: one with $\beta_F = 120$ and the other with $\beta_F = 150$. If all other transistor parameters and external components are matched, determine the resulting input offset voltage.

6.37. Find the current gain stability factor, S_β, for the Wilson current source using matched BJTs.

6.38. Find the current gain stability factor, S_β, for the Widlar current source using matched BJTs.

6.39. A BJT Widlar current source is designed for a load current of 100 μA using identical transistors with $\beta_F = 150$ and $V_A = 150$ V. If the fabrication process guarantees a $\beta_F = 150 \pm 10$, what is the resulting maximum deviation in load current from the original design?

6.40. A BJT Wilson current source is designed for a load current of 100 μA using identical transistors with $\beta_F = 150$ and $V_A = 150$ V. If the fabrication process guarantees a $\beta_F = 150 \pm 10$, what is the resulting maximum deviation in load current from the original design? Compare with the results of the previous problem and comment on the benefits of each design.

6.41. Design a BJT differential amplifier that uses a Widlar current source that amplifies a differential input signal of 0.25 V to provide a differential output signal of 5 V with differential input resistance of greater than 50 kΩ. Limit the signal amplitude across each base-emitter junction to 5 mV to insure linear operation. The BJTs are matched and have the following characteristics:

$$\beta_F = 200 \qquad \text{and} \qquad V_A = 170\,\text{V}.$$

Confirm the analytical design with SPICE.

6.42. Consider the BJT differential amplifier in Example 6.4. Determine the largest input common-mode signal that can be applied to the amplifier with the BJTs remaining in the linear region of operation.

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[2] ——-, *Bipolar Power Transistor Data Book*, 7th. Ed., Motorola, Inc., Phoenix, 1992

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CHAPTER 7

Power Amplifiers and Output Stages

In general, analog amplifiers discussed in the previous chapters are described as small-signal circuits whose purpose is to increase the amplitude of the input signal or act as an impedance buffer between other amplifier stages. In reality, these amplifiers accept signals over a broad range of amplitudes. This chapter describes amplifiers (or amplification stages) that are capable of delivering high power levels at the output.

Power amplifiers must be capable of delivering a specific amount of power to a load, such as a stereo amplifier to a pair of speakers or a radio frequency amplifier to a broadcasting antenna. They are also used as output stages in integrated circuits. Because high output powers may be involved, the efficiency of the amplifier to convert a low-power signal to high power becomes increasingly important. Inefficiency causes unwanted increases in transistor operating temperature and may lead to accelerated device failure. Because power amplifier stages may deliver high output power to low impedance loads, they are significantly different from the low- power small-signal amplifiers.

The large signal nature of power amplifiers warrants special design considerations that may not be significant for small-signal amplifiers. Therefore, small-signal approximations and models either are not appropriate or must be used with care. In large-signal operation, signals transverse the extremes of the forward-active region of the transistor causing distortion at the output. That is, when a pure sinusoid is introduced to a power amplifier, the output may no longer be a pure sinusoid, but a signal composed of the original sinusoid (at some amplitude determined by the amplification) and its Fourier (harmonic) components. The relative amplitude of the fundamental component decreases with respect to the Fourier components as distortion increases.

Distortion is defined in one of several ways depending on the particular application of the circuit. Measures of distortion include:

- Total harmonic distortion (THD) commonly used for audio circuits,
- Intermodulation distortion (IMD) using the two-tone ratio method for radio and microwave frequency circuits,
- Second- and third-order intercept points also used for radio and microwave circuits,
- Composite second-order (CSO) and composite third-order beat ratio (CTBR) used for cable television transmission circuits.

Description of the THD and IMD methods will be discussed, and the relationship between the two measurements will be presented.

The design and analysis concepts introduced in this chapter are:

- Analysis of distortion
- Design of large-signal (power) amplifiers with particular interest in reduction of distortion
- Thermal consideration that must be taken into account when designing power amplifiers.

7.1 POWER AMPLIFIER CLASSIFICATION

In previous chapters, amplifiers were classified in terms of their circuit configurations (common-emitter, common-collector, common-base, common-drain, common-source, and common-gate). Another classification scheme is used when classifying power amplifiers. This scheme labels circuits according to the portion of the period of the output waveform during which the transistors conduct. The measure of designation is the conduction angle of each transistor in the circuit, assuming a sinusoidal input.

Regardless of the classification of the power amplifier, it must be capable of handling large signal amplitudes where the current and voltages swings may be a significantly large fraction of the bias values. In such cases, small-signal analysis and models may not be appropriate and large signal (DC) transfer characteristics must be used. The limitation on small-signal operation is discussed in this section.

7.1.1 CLASSIFICATION SCHEME

The amplifier classifications by conduction angle for sinusoidal inputs are shown in Table 7.1. The output (collector or drain) current through a transistor for class A, B, AB, and C power amplifiers are shown in Figure 7.1. In Figure 7.1a, the current flows through the transistor over the whole period: this is classified as Class A operation. In Class B operation, shown in Figure 7.1b, each transistor only conducts over half the period of the input sinusoidal waveform. Class AB operation, shown in Figure 7.1c, illustrates current flow through each transistor for greater than a half cycle but less than the full cycle of the input sinusoid. Figure 7.1d shows Class C operation where the each transistor conducts over less than half cycle of the input sinusoid. Class D operation is not shown since the conduction angle could vary with time over the entire cycle.

Initially, it may seem as if Class A operation is the only configuration that will yield low distortion signals. Class B and class AB power amplifiers assure signal continuity by making use of arrangements of two transistors that allow each transistor to share portions of the input signal conduction angle. Class C amplifiers provide single-frequency sinusoidal output by driving resonant circuits over a small portion of the cycle; the continuity of the sinusoidal output is assured by the tuned circuit.[1] In Class D operation, there are two inputs, the input signal and a sampling

[1]Class C amplifiers are used for narrow-band signal applications. The focus of this section is on broad-band amplifiers.

Table 7.1: Amplifier classifications

Amplifier Class	Individual Transistor Conduction Angle
A	360˚
B	180˚
AB	180˚ - 360˚
C	Fixed drive, < 180˚
D	Switched operation, conduction angle may vary with time from 0˚ - 360˚ or may be fixed.

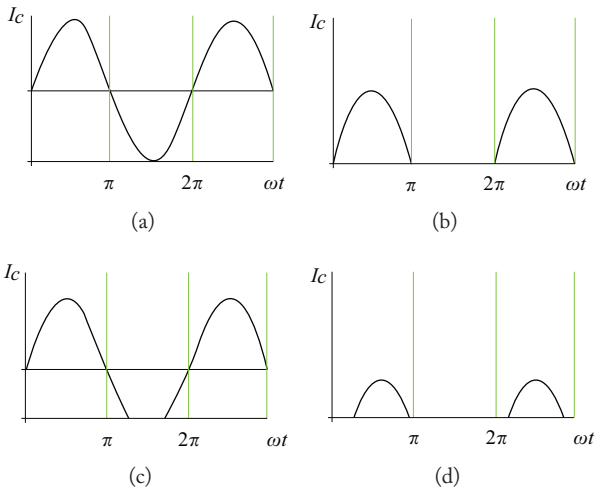


Figure 7.1: Transistor current for various amplifier classes: (a) Class A amplifier, full period current flow; (b) Class B amplifier, half period current flow; (c) Class AB amplifier, greater than half period current flow; (d) Class C amplifier, less than half the period current flow.

square wave or pulse width modulated signal. In essence, the sampling signal forces the transistors to either turn on or off over the interval of the sampling wave, yielding a sampled version of the input signal. This sampled signal is then filtered to yield the desired waveform.

Class A, B, and AB are studied in some detail in this Sections 7.2, 7.3, and 7.4, respectively. Class C and D amplifiers are not discussed since their analysis is beyond the scope of this book.

7.1.2 LIMITS ON DISTORTIONLESS "SMALL-SIGNAL" OPERATION

To investigate the limitations of analyses using small-signal models, the limiting mechanisms must be understood. Graphical method load-line analysis demonstrates the large-signal nature of

power amplifiers. The power amplifier is assumed to operate with large current and voltage swings which may be a significant fraction of its quiescent current and voltage.

As an example, consider a simple common-emitter power amplifier as shown in Figure 7.2.[2] The input and output characteristics are shown in Figure 7.3.

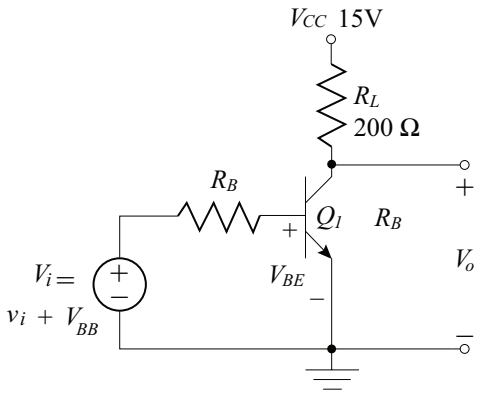


Figure 7.2: Common-emitter power amplifier.

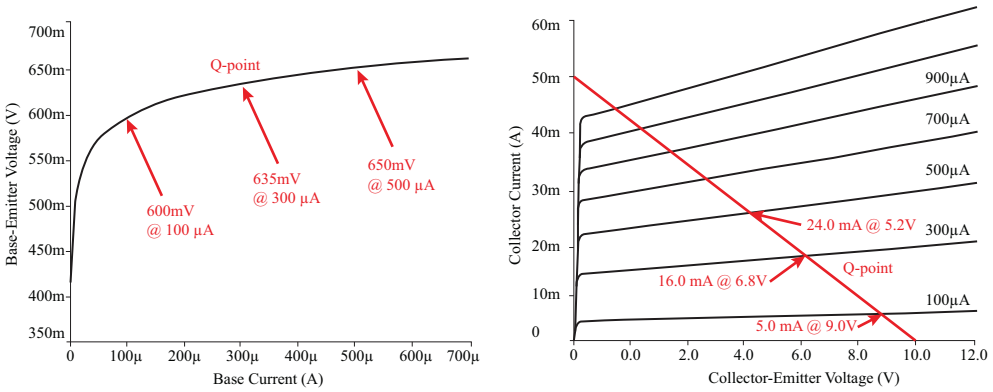


Figure 7.3: Characteristics of the common-emitter power amplifier of Figure 7.2: (a) Input characteristics; (b) Output characteristics.

The common-emitter power amplifier shown in Figure 7.2 has the following quiescent conditions: $I_{BQ} = 300\,\mu\text{A}$, $V_{BEQ} = 0.635\,\text{V}$, $I_C = 16\,\text{mA}$, and $V_{CEQ} = 6.8\,\text{V}$. For a large swing on the base current of $\pm 200\,\mu\text{A}$, the base-emitter voltage swings from 0.60 V to 0.65 V as shown

[2]This analysis is for demonstration purposes only: the simulations used a MJE340 BJT. Analysis of other BJT amplifier configurations and FET amplifier configurations can be performed in a similar fashion.

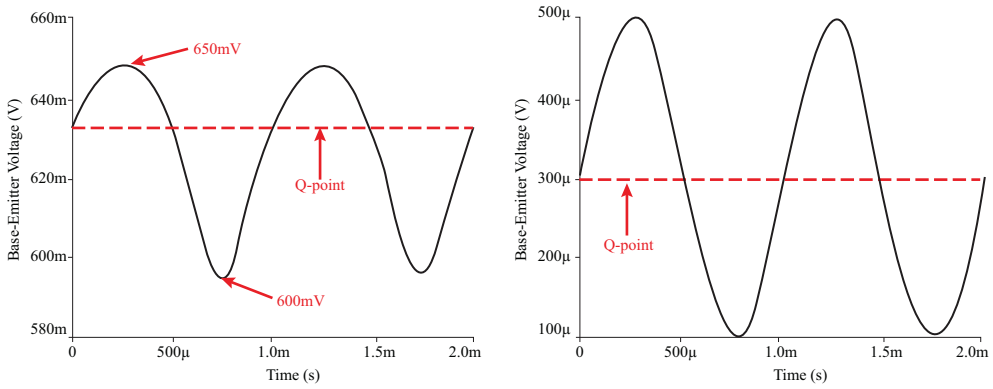


Figure 7.4: Input voltage and current waveforms for the power amplifier of Figure 7.2: (a) The base-emitter voltage; (b) base current (pure sinusoid).

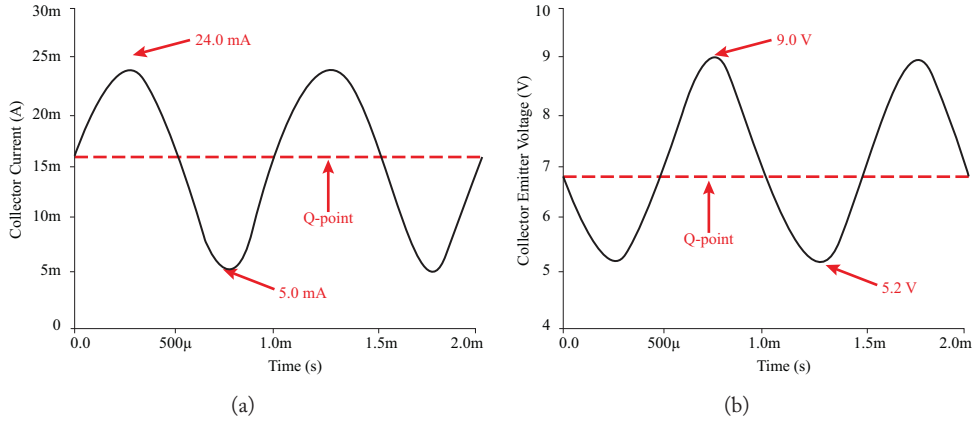


Figure 7.5: Output voltage and current waveforms for the power amplifier of Figure 7.2: (a) collector current; and (b) collector-emitter voltage.

in the input characteristics. The result is an asymmetric base-emitter voltage excursion about the operating point of $-0.035\,\text{V}$ and $+0.015\,\text{V}$. The output characteristics shows a corresponding swing in collector currents of 5 mA to 24 mA; resulting in an asymmetric current excursion about the operating point of $-11\,\text{mA}$ and $+8\,\text{mA}$.

The voltage and current waveforms can be obtained from the dynamic operating curves of Figure 7.3 and is shown in Figures 7.4 and 7.5. For a pure sinusoidal input base current, the base-emitter voltage, collector current, and collector-emitter voltage waveforms are shown to be

suffering from varying degrees of distortion. From the output characteristics, the collector-emitter voltage waveform has a quiescent value of 6.8 V and has a voltage swing from 5.2 V to 9.0 V. The output excursions about the operating point is −1.6 V and +3.8 V which is clearly asymmetrical.

For small-signal operation, the input signal is small which yields negligible distortion of the output waveform. In power amplifiers, however, the output signals are large and potentially distorted. Therefore, simple linear small-signal analysis cannot necessarily be used effectively. Instead, large-signal transfer characteristics are best used to determine the operating characteristics of the power amplifier.

The limit of distortionless "small-signal" analysis is difficult to define since it is dependent on amplifier distortion specifications. However, some sense of the limitation of small-signal analysis can be found by determining the relationship between the base-emitter voltage swing and the output current.

Assume that the base-emitter voltage is

$$V_{BE} = v_{be} + V_{BEQ}, \tag{7.1}$$

where

$$\begin{aligned} V_{BEQ} &= \text{quiescent base-emitter voltage (DC)}, \\ v_{be} &= \text{AC component of the base-emitter voltage} \\ &= V_1 \cos \omega t. \end{aligned} \tag{7.2}$$

From the Ebers-Moll equations (Equation 3.3 (Book 1)), the emitter current is

$$I_E = -I_{ES}\left(e^{\frac{v_{BE}}{\eta V_t}} - 1\right) + \alpha_R I_{CS}\left(e^{\frac{v_{BC}}{\eta V_t}} - 1\right), \tag{7.3}$$

where the base-emitter is defined by Equation (7.1).

For a strongly forward-biased transistor, $V_{BE} \gg \eta V_t$ and $V_{BC} \ll -\eta V_t$. Equation (7.3) can be simplified to

$$I_E \approx -I_{ES} e^{\frac{v_{BE}}{\eta V_t}} = -I_{ES} e^{\frac{V_{BE}}{\eta V_t}} e^{\frac{V_1 \cos \omega t}{\eta V_t}} = -I_{ES} e^{\frac{V_{BE}}{\eta V_t}} e^{x \cos \omega t}, \tag{7.4}$$

where $x = V_1/\eta V_t$ to normalize the drive voltage.

It is apparent from Equation (7.4) that the emitter current and, in turn, the collector current of the transistor in Figure 7.1 are proportional to the normalized ratio of $e^{x \cos \omega t}/e^x$ for any fixed value of x. Figure 7.6 shows the normalized emitter current (proportional to the collector current) as a function of time over two cycles of the variation in the base-emitter voltage. The plot clearly shows that by the time $x = 10$, the emitter current is clearly distorted. Small-signal analysis can still be used under these circumstances, but will not identify the distortion contained in the output signal.

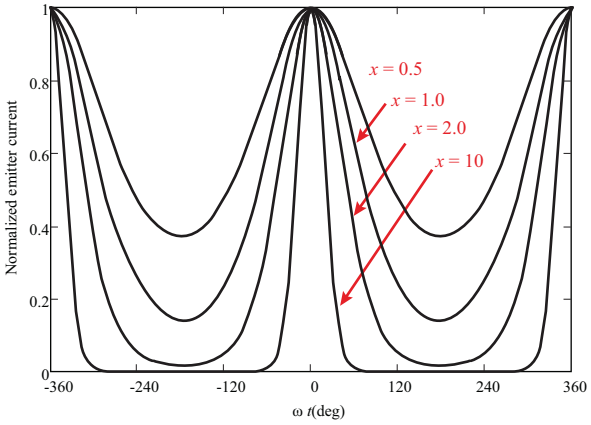


Figure 7.6: Normalized emitter current vs. angle for varying base-emitter voltages.

7.2 CLASS A POWER AMPLIFIERS

7.2.1 COMMON-COLLECTOR

Consider a common-collector power amplifier driven by a voltage V_i, shown in Figure 7.7. The linear BJT models of Figure 3.8 (Book 1)) for the cutoff, forward-active, and saturation regions are used to find the large signal transfer function for the common-collector power amplifier.

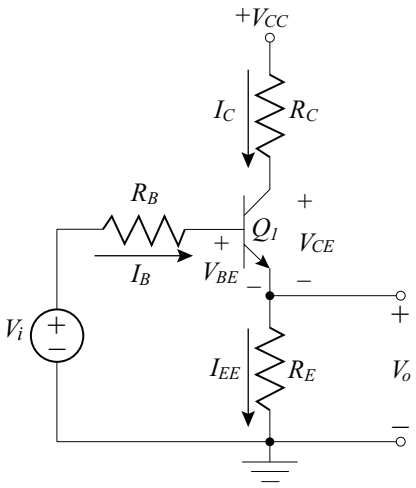


Figure 7.7: Common-collector power amplifier.

The power amplifier in Figure 7.7 is re-drawn using the equivalent models for the cutoff, forward-active, and saturation regions in Figure 7.8.

The transistor Q_1 is cutoff when $V_{BE} < V_{BE(on)}$. No current flows through Q_1, effectively creating an open circuit at the emitter, base, and collector nodes as shown in Figure 7.8a. Therefore, $V_O = 0$ until the transistor turns on with $V_i > V_{BE(on)}$. Recall that a typical value of $V_{BE(on)}$ for silicon transistors is 0.6 V.

When Q_1 turns on, the transistor operates in the forward-active region and the amplifier is modeled as shown in Figure 7.8b. The output voltage is,

$$V_O = I_{EE} R_E, \tag{7.5}$$

where $I_{EE} = -I_E$.

The base-emitter loop equation is written to find I_{EE} in terms of V_i,

$$\begin{aligned} 0 &= V_i - I_B R_B - V_\gamma - I_{EE} R_E \\ &= V_i - \frac{I_{EE}}{\beta_F + 1} R_B - V_\gamma - I_{EE} R_E. \end{aligned} \tag{7.6}$$

Solving for I_{EE} yields,

$$I_{EE} = \frac{(\beta_F + 1)(V_i - V_\gamma)}{R_B + (\beta_F + 1) R_E}. \tag{7.7}$$

The transfer function is found by substituting Equation (7.7) into (7.5):

$$V_O = I_{EE} R_E = \left[\frac{(\beta_F + 1)(V_i - V_\gamma)}{R_B + (\beta_F + 1) R_E} \right] R_E, \tag{7.8}$$

where the slope of the transfer function in the forward active region is $(\beta_F + 1) R_E / R_B + (\beta_F + 1) R_E$.

In saturation, the amplifier is modeled as shown in Figure 7.8c. The typical collector-emitter voltage is $V_{CE(sat)} = 0.2$ V and the base-emitter voltage is $V_{BE(sat)} = 0.6$ V. It is useful to redraw the circuit in Figure 7.8c to analyze this case, as shown in Figure 7.9.

The transfer function for the saturation model of the common-collector amplifier is easily found by applying the superposition principle to Figure 7.9,

$$\begin{aligned} V_O &= \frac{V_i (R_E // R_C)}{R_B + (R_E // R_C)} - \frac{V_{BE(sat)} (R_E // R_C)}{R_B + (R_E // R_C)} - \frac{V_{CE(sat)} (R_B // R_E)}{R_C + (R_B // R_E)} + \frac{V_{CC} (R_B // R_E)}{R_C + (R_B // R_E)} \\ &= \frac{(V_i - V_{BE(sat)})(R_E // R_C)}{R_B + (R_E // R_C)} + \frac{(V_{CC} - V_{CE(sat)})(R_B // R_E)}{R_C + (R_B // R_E)}. \end{aligned} \tag{7.9}$$

The large-signal gain, V_O / V_i, is proportional to $(R_E // R_C) / [R_B + (R_E // R_C)]$.

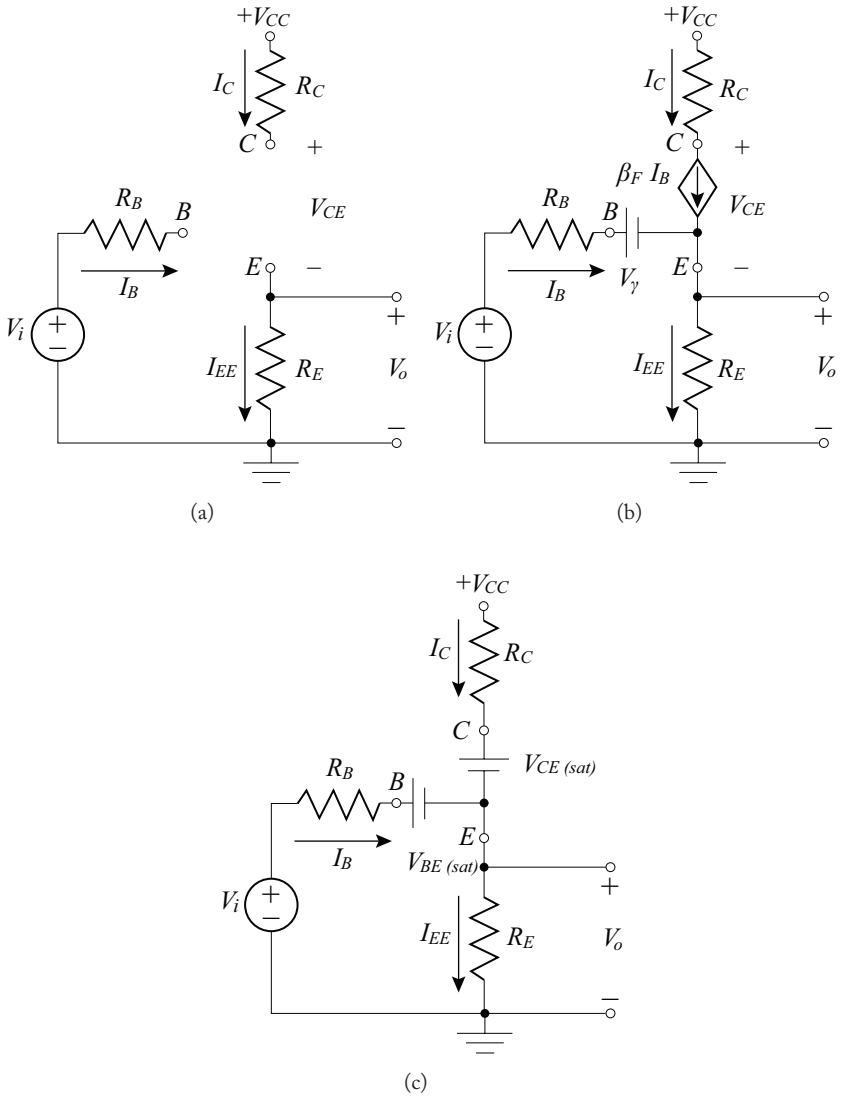


Figure 7.8: Equivalent models for the (a) cutoff, (b) forward-active, and (c) saturation regions for the common-emitter power amplifier in Figure 7.7.

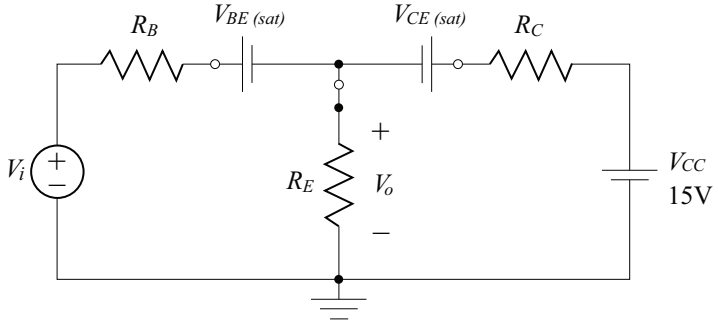


Figure 7.9: Re-drawn saturation model of the power amplifier in Figure 7.8c.

The boundary between the forward-active and cutoff regions can be found by solving the collector-emitter loop equation using the forward-active model of the circuit:

$$V_{CE(sat)} = V_{CC} - I_C R_C - I_{EE} R_E. \tag{7.10}$$

But

$$I_C = \frac{\beta_F}{\beta_F + 1} I_{EE} \qquad \text{and} \qquad I_{EE} = (\beta_F + 1) I_B \qquad \text{so,}$$

$$V_{CE(sat)} = V_{CC} - I_{EE}\left(\frac{\beta_F}{\beta_F + 1} R_C + R_E\right). \tag{7.11}$$

The value for V_i at the boundary between the forward-active and saturation regions is found by substituting Equation (7.7) into (7.11) and rearranging the equation,

$$V_{i(f-a/sat)} = \frac{(V_{CC} - V_{CE(sat)})[R_B + (\beta_F + 1)R_E]}{[(\beta_F + 1)R_E + \beta_F R_C]} + V_{BE(sat)}. \tag{7.12}$$

To find the output voltage at the forward-active and saturation region boundary, substitute Equation (7.12) into (7.8) to yield

$$V_{O(f-a/sat)} = \frac{(\beta_F + 1)(V_{CC} - V_{CE(sat)})}{[(\beta_F + 1)R_E + \beta_F R_C]} R_E. \tag{7.13}$$

A typical transfer characteristic of the circuit in Figure 7.7 is shown in Figure 7.10.

The transfer characteristic in Figure 7.10 indicates that when the input voltage exceeds $V_{i(f-a/sat)}$ then the output voltage of the common-collector power amplifier will begin to "clip" and distort the output. The output will also "clip" when the input voltage is less than V_{BE}.

If the common-collector amplifier is operating in the "linear" region of the large signal transfer characteristic, it may be assumed that there is little nonlinear distortion. In this case, the power and efficiency calculations are straightforward.

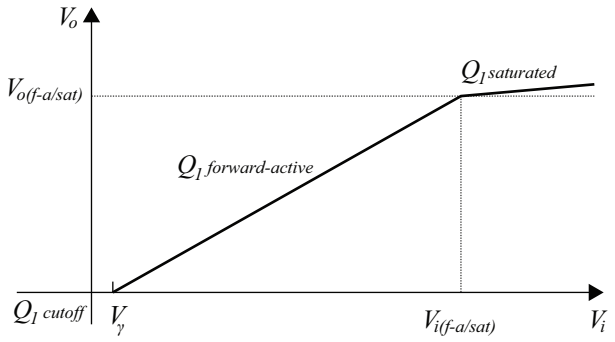


Figure 7.10: Transfer characteristic of the common-collector power amplifier in Figure 7.7.

Recall that because power amplifiers may be required to deliver large currents and voltages at the output, the conversion efficiency of the circuit is of interest. That is, higher efficiency power amplifiers will produce higher output power signals at the same amount of applied dc power than lower efficiency power amplifiers.

The DC power that the amplifier requires from the power supply is,

$$P_{DC} = V_{CC} I_{CQ}. \tag{7.14}$$

The AC power output of the common-collector amplifier is found by multiplying the root-mean-squared (rms) values of the load current and voltage in terms of the peak values,

$$P_{AC} = \frac{I_{EP}}{\sqrt{2}} \frac{V_{EP}}{\sqrt{2}} = \frac{I_{EP}^2 R_E}{2} = \frac{V_{EP}^2}{2R_E}, \tag{7.15}$$

where

$$\begin{aligned} I_{EP} &\equiv \text{ the peak emitter current} \\ V_{EP} &\equiv \text{ the peak excursion from the quiescent voltage,} \end{aligned} \tag{7.16}$$

and $V_{EP} = V_{O(f-a/sat)}$ and $I_{EP} = V_{O(f-a/sat)}/R_E$ referred to Figures 7.7 and 7.10.

The rms values of the peak emitter current and voltage are found from their maximum and minimum values,

$$\frac{I_{EP}}{\sqrt{2}} = \frac{1}{\sqrt{2}} \frac{I_{E,\max} - I_{E,\min}}{2} \tag{7.17}$$

$$\frac{V_{EP}}{\sqrt{2}} = \frac{1}{\sqrt{2}} \frac{V_{E,\max} - V_{E,\min}}{2}. \tag{7.18}$$

The peak values of the emitter current and voltage are shown in Figure 7.11.

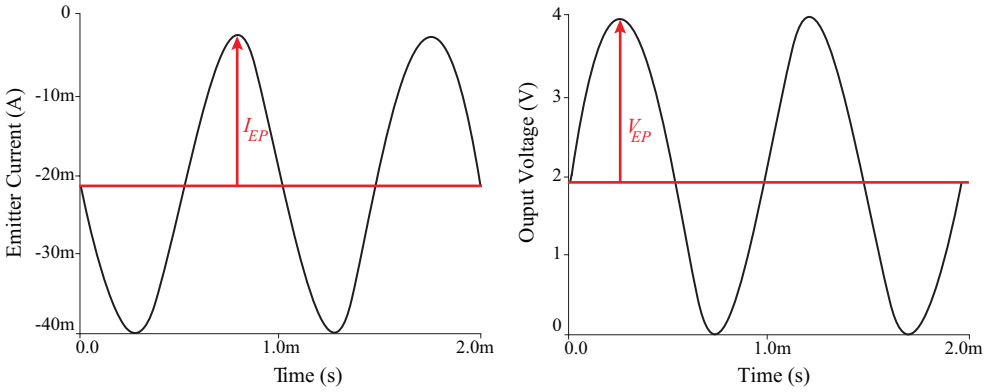


Figure 7.11: Peak values of the (a) emitter current and (b) emitter (load) voltage derived from the current and voltage waveforms.

The AC power in terms of the peak current and voltage values are,

$$P_{AC} = \frac{I_{EP}V_{EP}}{2} = \frac{(I_{E,\max} - I_{E,\min})(V_{E,\max} - V_{E,\min})}{8}. \tag{7.19}$$

The conversion efficiency of the applied DC power to the total AC power is defined as,

$$\eta = \frac{\text{AC power delivered to load}}{\text{DC power supplied}} \times 100\% = \frac{P_{AC}}{P_{DC}} \times 100\%. \tag{7.20}$$

Substituting Equations (7.19) and (7.14) into (7.20) yields an expression for the conversion efficiency of the common-collector power amplifier in terms of the maximum and minimum values of the output current and voltage,

$$\eta = \frac{(I_{E,\max} - I_{E,\min})(V_{E,\max} - V_{E,\min})}{8V_{CC}I_{CQ}} \times 100\%. \tag{7.21}$$

For *maximum* attainable ideal efficiency for the common-collector power amplifier configuration, the output current and voltage is set to its extremes. That is,

$$\begin{aligned} I_{E,\min} &= 0 \quad I_{E,\max} = 2I_{EQ} \\ V_{E,\min} &= 0 \quad V_{E,\max} = V_{CC} - V_{CE(sat)}, \end{aligned}$$

for $V_{CC} - V_C = 0$.

The maximum attainable efficiency is for large β,

$$\begin{aligned}\eta_{\max} &= \frac{P_{AC}}{P_{DC}} \times 100\% = \frac{I_{EP}V_{EP}}{2(V_{CC}I_{CQ})} \times 100\% \\ &= \frac{\left(\frac{2I_{EQ}}{2}\right)\left(\frac{V_{CC}-V_{CE(sat)}}{2}\right)}{2(V_{CC}I_{CQ})} \times 100\% \approx 25\%,\end{aligned} \tag{7.22}$$

where $V_{CC} \gg V_{CE(sat)}$.

Naturally, the power amplifier shown in Figure 7.7 will never be able to reach an efficiency of 25% for finite values of R_C which lowers the peak output current and voltage.

Example 7.1

The common-collector power amplifier shown in Figure 7.7 has the following circuit element and transistor parameter values:

$$\begin{aligned} V_{CC} &= 15\,\text{V} \quad R_C = 100\,\Omega \quad R_E = 100\,\Omega \\ R_B &= 10\,\text{k}\Omega \quad \beta_F = 160. \end{aligned}$$

Determine the maximum efficiency of the power amplifier assuming no additional losses due to thermal effects.

Solution:

From Equation (7.20), the efficiency is

$$\eta = \frac{P_{AC}}{P_{DC}} \times 100\%.$$

But from Equation (7.15),

$$P_{AC} = \frac{V_{EP}^2}{2R_E} = \frac{1}{2R_E}\left[\frac{(V_{O(f-a/sat)}-0)}{2}\right]^2 = \frac{V_{O(f-a/sat)}^2}{8R_E}.$$

The power delivered by the power supply is related to the peak output voltage by,

$$P_{DC} = V_{CC}I_{CQ} = V_{CC}\left[\left(\frac{\beta_F}{\beta_F+1}\right)\frac{V_{O(f-a/sat)}}{2R_E}\right].$$

The efficiency is then

$$\eta = \frac{\frac{V_{O(f-a/sat)}^2}{8R_E}}{V_{CC}\left[\left(\frac{\beta_F}{\beta_F+1}\right)\frac{V_{O(f-a/sat)}}{2R_E}\right]} = \frac{\beta_F+1}{\beta_F}\frac{V_{O(f-a/sat)}}{4V_{CC}}.$$

Substituting Equation (7.13) for the maximum output voltage in to the expression for efficiency above yields,

$$\eta = \frac{(\beta_F + 1)}{\beta_F} \left\{ \frac{\dfrac{(\beta_F + 1)(V_{CC} - V_{CE(sat)})}{[(\beta_F + 1)R_E + \beta_F R_C]} R_E}{4V_{CC}} \right\}$$

$$= \frac{161}{160} \left\{ \frac{\dfrac{161(15 - 0.2)(100)}{(161)(100) + (160)(100)}}{(4)(15)} \right\} \times 100\% = 12.5\%.$$

As expected, the efficiency for the common-collector power amplifier of Figure 7.7 with the circuit values of this example is less than the ideal maximum efficiency of 25%.

Integrated circuits also use power output stages for their low distortion and low output resistance characteristic. Consider the common-collector circuit biased by a current mirror shown in Figure 7.12. Like its discrete counterpart, when this circuit is to be used as the output amplifier stage in an integrated circuit, it must be capable of handling large signal amplitudes where the current and voltages swings may be a significantly large fraction of the bias values. In such cases, small signal analysis and models may not be appropriate and large signal (DC) transfer characteristics must be used.

In the circuit of Figure 7.12, Q_2, Q_3, and R_B forms a current mirror to bias the common-collector circuit formed by Q_1. The large signal transfer characteristic is

$$V_O = V_i - V_{BE\,1}, \tag{7.23}$$

where $V_O = I_O R_L$. Using the simplified Ebers-Moll emitter current expression in Equation 3.3 (Book 1) when Q_1 is forward biased,

$$I_{E1} \approx -I_{ES} \left(e^{\dfrac{V_{BE1}}{\eta V_t}} - 1 \right) \approx -I_{ES} e^{\dfrac{V_{BE1}}{\eta V_t}}. \tag{7.24}$$

But

$$-I_{E1} = I_Q + \frac{V_O}{R_L}, \tag{7.25}$$

when Q_2 is in the forward active region.

Solving for V_{BE1} by substituting Equation (7.25) in to (7.24) yields,

$$V_{BE1} = \eta V_t \ln \left(\frac{I_Q + \frac{V_O}{R_L}}{I_{ES}} \right). \tag{7.26}$$

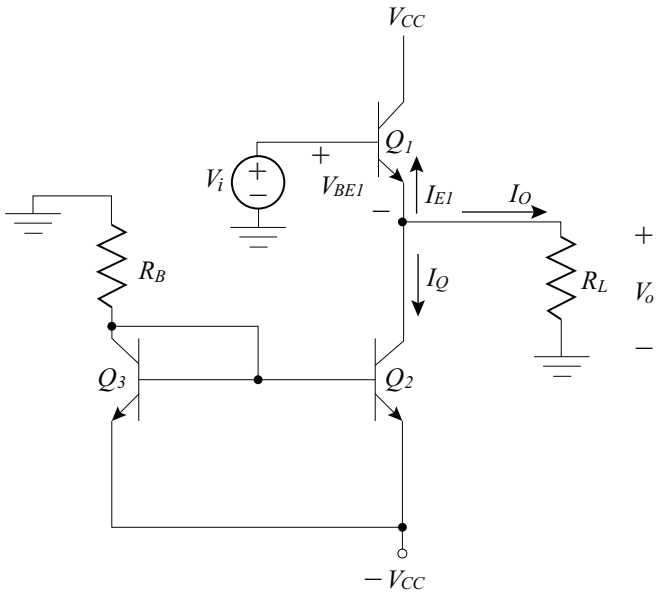


Figure 7.12: Common-collector power amplifier biased by a current mirror (formed by Q_2, Q_3, and R_B).

By substituting Equation (7.26) into (7.23), a nonlinear equation for the transfer function is found under the assumption that the load resistor R_L is small when compared to the output resistance of the transistors,

$$V_O = V_i - \eta V_t \ln\left(\frac{I_Q + \frac{V_O}{R_L}}{I_{ES}}\right), \tag{7.27}$$

or

$$V_i = \eta V_t \ln\left(\frac{I_Q + \frac{V_O}{R_L}}{I_{ES}}\right) + V_O. \tag{7.28}$$

Equation (7.28) is a transfer function for the common-collector power amplifier and its transfer characteristics are plotted in Figure 7.13 for $\eta = 1$.

Referring to the transfer characteristic shown in Figure 7.13, consider the case when the load resistor is large (designated $R_{L-large}$). When the load resistor is large, the natural logarithm in Equation (7.28) remains relatively constant with changing V_O. Physically, this means that for large load resistors, the current in the load is small and that $I_{E1} \approx I_Q$. This also implies that V_{BE1} is approximately constant. Therefore, when both Q_1 and Q_2 are in the forward active region, the transfer characteristic for $R_{L-large}$ is nearly a straight line offset by the quiescent base-emitter voltage V_{BEQ1} on the V_i axis.

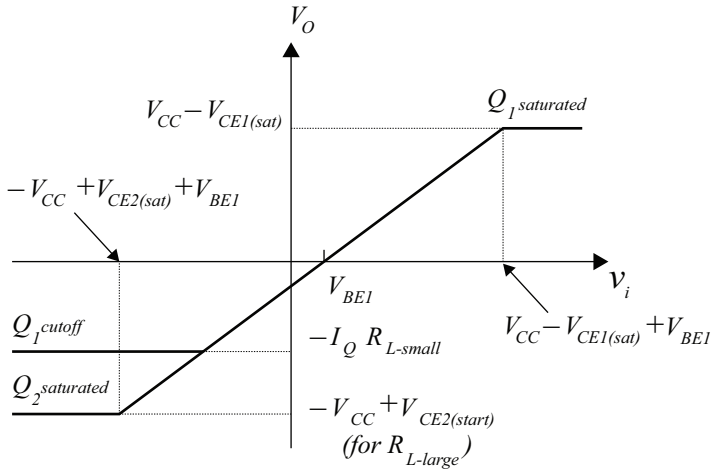


Figure 7.13: Transfer characteristic of the common-collector power amplifier of Figure 7.12.

As V_i is made a large positive input, the Q_1 collector-base junction is forward biased and saturates the transistor so that the output is,

$$V_{O(\max)} = V_{CC} - V_{CE1(sat)}, \tag{7.29}$$

where the input voltage is:

$$V_{i(\max)} = V_{CC} - V_{CE1(sat)} + V_{BE1}. \tag{7.30}$$

When V_i is made large and negative, Q_2 saturates and the output voltage is,

$$V_{O(\min)} = -V_{CC} + V_{CE2(sat)}, \tag{7.31}$$

where the input voltage is,

$$V_{i(\max)} = -V_{CC} + V_{CE2(sat)} + V_{BE1}. \tag{7.32}$$

For a large and negative input voltage with small values of the load resistance, $R_{L-small_1}$, the natural logarithm in Equation (7.28) approaches negative infinity at

$$V_O = -I_Q R_{L-small}. \tag{7.33}$$

In this case, the load current is equal to I_Q. Therefore, no current flows in Q_1, sending it into cutoff. Then V_O no longer increases with V_i.

For a large positive input voltage with $R_{L-small}$, the transfer characteristic is similar to the case for $R_{L-large}$.

The maximum efficiency of the current source biased common-collector output stage is also 25%.

7.2.2 COMMON-EMITTER

Common-emitter power amplifier stages are frequently used as output stage drivers of multi-transistor amplifiers. However, common-emitter output stages are not often used in integrated circuit design because of the superior characteristics of the common-collector stages (low output resistance and low distortion).

Consider a common-collector power amplifier driven by a voltage V_i, shown in Figure 7.13. As in the common-collector power amplifier analysis, the linear BJT models of Figure 3.8 (Book 1)for the cutoff, forward-active, and saturation regions are used to find the large signal transfer function for the common-collector power amplifier.

The common-emitter power amplifier in Figure 7.14 is analyzed in the same way as the common-collector configuration using the equivalent models for the cutoff, forward-active, and saturation regions.

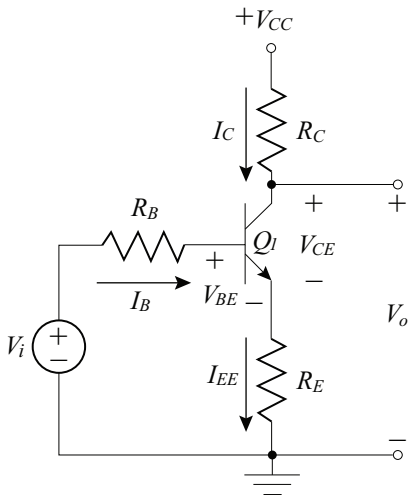


Figure 7.14: Common-emitter power amplifier.

Transistor Q_1 does not conduct until the base-emitter voltage is $V_{BE(on)} \approx 0.6\,\text{V}$. Since Q_1 is in cutoff, the V_i must exceed $V_{BE(on)}$ for the transistor to enter the forward-active region. The output voltage at this point in the transfer characteristic is $V_O = V_{CC}$.

In the forward-active region, the output voltage is

$$V_O = V_{CC} - \frac{R_C(V_i - V_\gamma)}{\left[\frac{R_B}{\beta_F} + \left(\frac{\beta_F}{\beta_F + 1}\right) R_E\right]}. \tag{7.34}$$

In the saturation region, the output voltage of the common-emitter is

$$V_O = \frac{(V_i - V_{BE(sat)})(R_E//R_C)}{R_B + (R_E//R_C)} + \frac{V_{CE(sat)}R_C + V_{CC}(R_E//R_B)}{R_C + (R_E//R_B)}. \tag{7.35}$$

The transfer characteristic is shown in Figure 7.15.

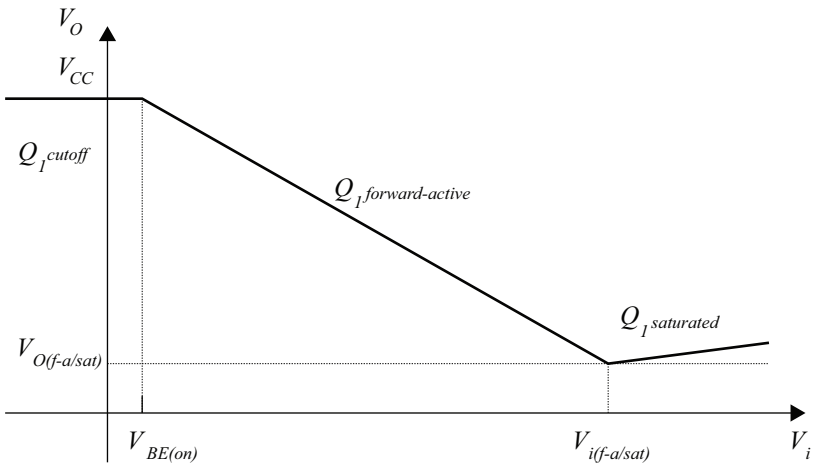


Figure 7.15: Transfer characteristic of the common-emitter power amplifier in Figure 7.14.

The AC power output of the common-emitter amplifier is found by multiplying the root-mean-squared (rms) values of the load current and voltage in terms of the peak values,

$$P_{AC} = \frac{I_{CP}}{\sqrt{2}}\frac{V_{CP}}{\sqrt{2}} = \frac{I_{CP}^2 R_C}{2} = \frac{V_{CP}^2}{2R_C}, \tag{7.36}$$

where

$$\begin{aligned} I_{CP} &= \text{the peak collector current} \\ V_{CP} &= \text{the peak voltage from the collector to ground} \end{aligned} \tag{7.37}$$

and $V_{CP} = V_{CC}$ and $I_{CP} = (V_{CC} - V_{O(f-a/sat)})/R_C$ referred to Figure 7.15.

The RMS values of the peak emitter current and voltage are found from their maximum and minimum values,

$$\frac{I_{CP}}{\sqrt{2}} = \frac{1}{\sqrt{2}}\frac{I_{C,\max} - I_{C,\min}}{2} \tag{7.38}$$

$$\frac{V_{CP}}{\sqrt{2}} = \frac{1}{\sqrt{2}}\frac{V_{C,\max} - V_{C,\min}}{2}. \tag{7.39}$$

The AC power in terms of the peak current and voltage values are,

$$P_{AC} = \frac{I_{CP}V_{CP}}{2} = \frac{(I_{C,\max} - I_{C,\min})(V_{C,\max} - V_{C,\min})}{8}. \tag{7.40}$$

Substituting Equations (7.40) into (7.20) yields an expression for the conversion efficiency of the common-emitter power amplifier in terms of the maximum and minimum values of the output current and voltage,

$$\eta = \frac{(I_{C,\max} - I_{C,\min})(V_{C,\max} - V_{C,\min})}{8V_{CC}I_{CQ}} \times 100\%. \tag{7.41}$$

For *maximum* attainable ideal efficiency for the common-emitter power amplifier configuration, the output current and voltage is set to its extremes. That is,

$$\begin{aligned} I_{C,\min} &= 0 & I_{C,\max} &= 2I_{CQ} \\ V_{C,\min} &= V_{CE(sat)} & V_{C,\max} &= V_{CC}, \end{aligned}$$

for $V_E = 0$.

The maximum attainable efficiency is for large β_F,

$$\begin{aligned} \eta_{\max} &= \frac{P_{AC}}{P_{DC}} \times 100\% = \frac{I_{CP}V_{CP}}{2(V_{CC}I_{CQ})} \times 100\% \\ &= \frac{\left(\frac{2I_{CQ}}{2}\right)\left(\frac{V_{CC} - V_{CE(sat)}}{2}\right)}{2(V_{CC}I_{CQ})} \times 100\% \approx 25\%, \end{aligned} \tag{7.42}$$

where $V_{CC} \gg V_{CE(sat)}$.

Naturally, the power amplifier shown in Figure 7.14 will never be able to reach an efficiency of 25% for finite values of R_E which lowers the peak output current and voltage.

A common-emitter integrated circuit power output stage is shown in Figure 7.16. The transistor Q_2 is part of a constant current source that establishes the Q-point for transistor Q_1. The large signal characteristic is derived by first inspecting the load resistance node,

$$I_O = I_Q - I_{C1}. \tag{7.43}$$

The output voltage V_o is,

$$V_O = I_O R_L. \tag{7.44}$$

The collector current I_{C1}, for Q_1 assuming operation in the forward active region is found using Ebers-Moll Equation 3.3 (Book 1),

$$I_{C1} \approx \alpha_F I_{ES} e^{\frac{V_{BE1}}{\eta V_t}} = \frac{\beta_F}{\beta_F + 1} I_{ES} e^{\frac{V_{BE1}}{\eta V_t}}. \tag{7.45}$$

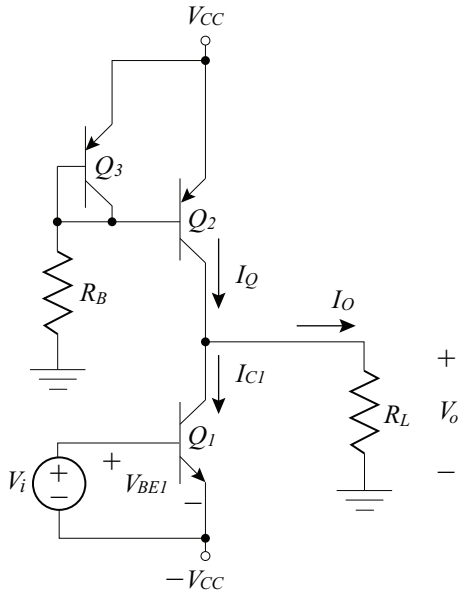


Figure 7.16: Common-emitter power amplifier biased by a current mirror (formed by Q_2, Q_3, and R_B).

But

$$I_{C1} = I_Q - \frac{V_O}{R_L}, \tag{7.46}$$

when Q_2 is in the forward active region.

Substituting Equation (7.46) in to (7.45) and knowing that $V_{BE1} = V_i$ yields,

$$\frac{\beta_F}{\beta_F + 1} I_{ES} e^{\frac{V_{BE1}}{\eta V_t}} = I_Q - \frac{V_O}{R_L}. \tag{7.47}$$

The output voltage is

$$V_O = -R_L \left(\frac{\beta_F}{\beta_F + 1} I_{ES} e^{\frac{V_{BE1}}{\eta V_t}} - I_Q \right). \tag{7.48}$$

If R_L is small, much off I_Q flows through the load when V_i is reduced. With V_i small or negative, the first term in the parenthesis in Equation (7.48) becomes negligible. Therefore, for $R_{L-small}$, the output voltage is,

$$V_O = I_Q R_{L-small}. \tag{7.49}$$

If R_L is large, V_o increases with decreasing V_i until Q_2 saturates. Therefore, for $R_{L-large}$,

$$V_O = V_{CC} - V_{CE2(sat)}. \tag{7.50}$$

For either small or large load resistance, as V_i increases and becomes more positive, I_Q increases and V_O becomes negative until Q_1 saturates.

Equation (7.48) is a nonlinear equation for the transfer function of the common-emitter amplifier biased by a current source in Figure 7.16 and is plotted in Figure 7.17 for $\eta = 1$.

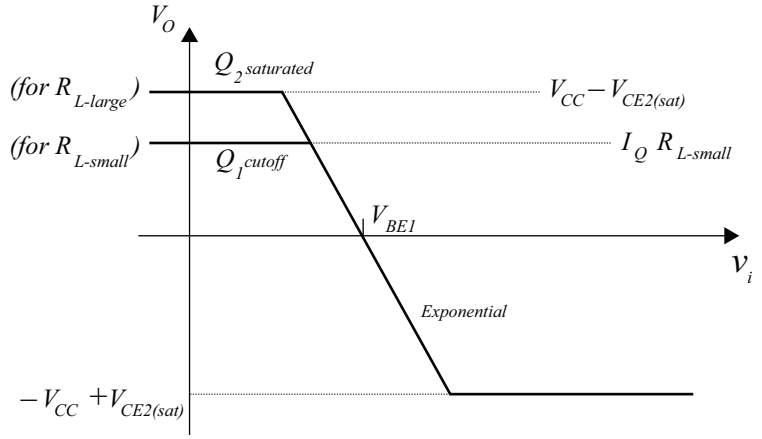


Figure 7.17: Transfer characteristic of the common-emitter power amplifier of Figure 7.16.

From Equation (7.48), the transfer function is an exponential. Therefore, the transfer characteristics shows a curvature. between the extreme output voltages. This causes distortion of the output signal that is significantly more pronounced than that of the common-collector amplifier of Figure 7.12. As in the common-collector power amplifier in Figure 7.12, the upper limit of the transfer function depends on the size of R_L.

The maximum efficiency of the current source biased common-emitter output stage is also 25%.

7.2.3 TRANSFORMER-COUPLED CLASS A POWER AMPLIFIER

If a load is connected directly to the transistor as in the common-emitter power amplifier in Figure 7.14, the quiescent current must pass through the load. The load increases the required DC power and reduces efficiency since the quiescent current through the load does not contribute to the AC signal component. To circumvent this problem, the load is commonly transformer coupled to the transistor as shown in Figure 7.18.

The transformer is used as an impedance matching element. To transfer a significant amount of power to a low impedance load, such as a the voice coil of a loudspeaker which is typically between 4 and 15 Ω, it is necessary to use an output matching transformer.

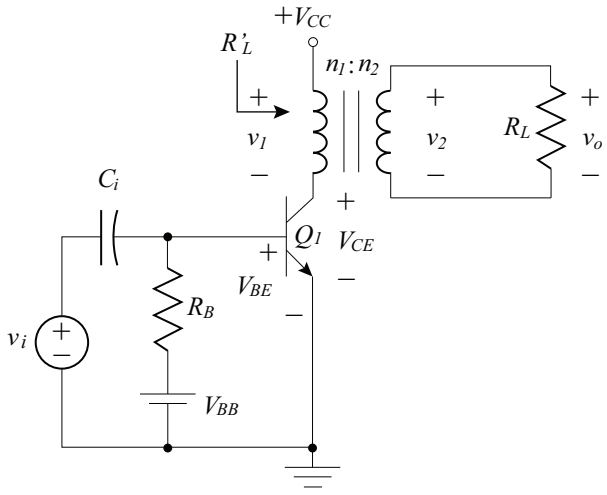


Figure 7.18: Class A power amplifier with a transformer coupled output.

For an ideal transformer, the AC voltage-current relations are,

$$v_1 = \frac{n_1}{n_2} v_2 \quad \text{and} \quad i_1 = \frac{n_2}{n_1} i_2, \tag{7.51}$$

where v_1 and v_2 are the voltages across the primary and secondary windings, respectively, and i_1 and i_2 are the currents through the primary and secondary windings, respectively. n_1 and n_2 are the number of turns in the primary and secondary, respectively, of the transformer.

Using Equation (7.50), the effective input resistance looking into the primary winding is

$$R'_L = \frac{v_1}{i_1} = \left(\frac{n_1}{n_2}\right)^2 R_L. \tag{7.52}$$

The DC and AC loadlines for the circuit in Figure 7.18 are shown on the output transistor characteristics in Figure 7.19.

The DC load line is nearly vertical due to the very small primary resistance in the transformer. If, however, a emitter resistor is present, the DC load line will have a slope of $-1/R_E$. The maximum peak-to-peak output voltage is $2V_{CC}$, and the maximum peak-to-peak output current is $2I_C$. Therefore, the maximum peak-to-peak AC power is,

$$P_{AC} = \frac{V_P I_P}{2} = \frac{V_{CC} I_C}{2}. \tag{7.53}$$

The maximum possible efficiency for a transformer coupled Class A power amplifier is,

$$\eta_{\max} = \frac{P_{AC}}{P_{DC}} \times 100\% = \frac{V_{CC} I_C}{2 V_{CC} I_C} \times 100\% = 50\%, \tag{7.54}$$

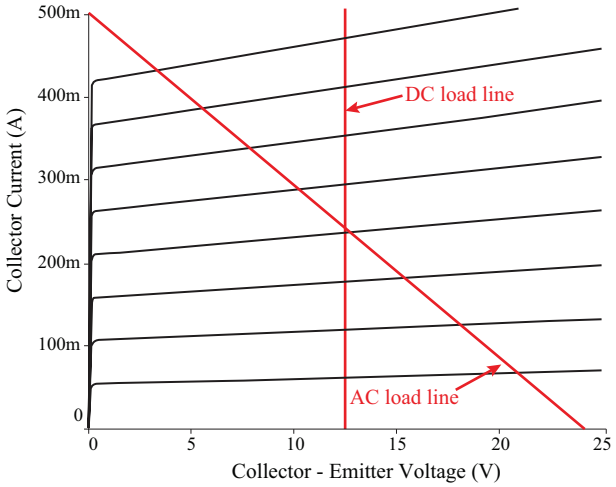


Figure 7.19: Output characteristics of the transformer-coupled Class A power amplifier shown in Figure 7.18.

which is double the maximum efficiency of Class A amplifiers that directly drives a load resistor. Naturally, the efficiency of real transformer coupled Class A power amplifiers will be lower than 50% due to additional losses (e.g., transformer losses).

Example 7.2
Using graphical techniques, design a transformer coupled Class A transistor amplifying stage to meet the following requirements:

Load Resistance:	2 kΩ
Output Transformer Efficiency:	67% (it's a BAD transformer)
Power output:	1 W (maximum, sinusoidal)
Temperature:	27°C
Supply Voltage:	12 V
Frequency:	400 Hz

A 2N6474 *npn* transistor is available with the following SPICE characteristic parameters:

IS = 2.45 pA	BF = 208	BR = 13
XTI = 3	XTB = 1.5	VAF = 100.

Solution:

From the specifications, the Class A amplifier may be assumed to enter the saturation and cutoff regions of the transistor characteristics for power delivery in excess of 1 W of full load power (P_{FL}).

Since the transformer efficiency is 67%, the amplifier stage must supply

$$P_{AC} = \frac{P_{FL}}{\eta_{xfmr}} = \frac{1.0}{0.67} = 1.5\,\text{W}.$$

Assume that the amplifier is configured identically to Figure 7.18.

The peak-to-peak collector current can be found by applying the expression for the AC power delivered and by considering the saturation region of the transistor:

$$P_{AC} = 1.5 = \frac{V_P}{\sqrt{2}}\frac{I_P}{\sqrt{2}}\left[\frac{\left(V_{CC} - \frac{1}{2}V_{CE(sat)}\right)}{\sqrt{2}}\right]\left[\frac{(2I_C)}{2\sqrt{2}}\right] = \frac{I_C\left(V_{CC} - \frac{1}{2}V_{CE(sat)}\right)}{2}.$$

Rearranging the equation above, solve for the maximum (peak-to-peak) collector current,

$$I_{C,\max} = 2I_C = \frac{4P_{AC}}{V_{CC} - \frac{1}{2}V_{CE(sat)}} = \frac{4(1.5)}{12 - .1} \approx 0.5\,\text{A}.$$

The peak-to-peak output voltage is,

$$V_{C,\max\,p-p} = 2V_{CC} - V_{CE(sat)}.$$

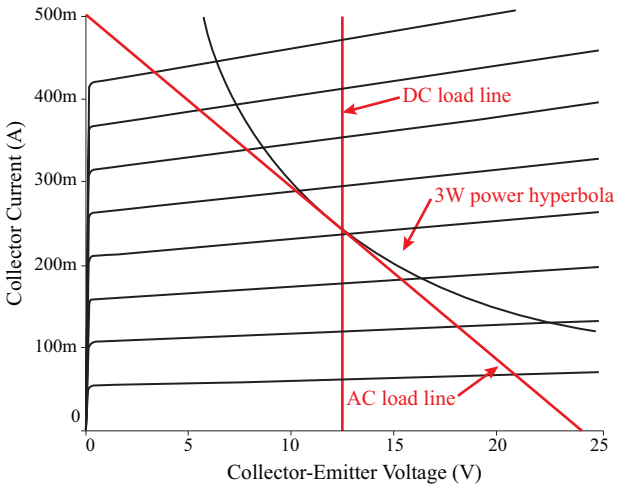
Therefore, the load seen by the transistor is,

$$R'_L = \frac{V_{C,\max\,p-p}}{I_{C,\max}} = \frac{2(12) - 0.2}{0.5} \approx 48\,\Omega.$$

The quiescent point is

$$V_{CE} = 12\,\text{V} \qquad I_C = 0.25\,\text{A},$$

resulting in a standby dissipation of $V_{CE}I_C = 3\,\text{W}$. The load line analysis is shown below.



The quiescent base current is approximately $I_B = 1.1\,\text{mA}$. Also drawn on the load line graph is the 3 W constant power dissipation hyperbola. A rough calculation may be made to determine the base bias resistor R_{BB}. Assuming that $V_{BB} = V_{CC}$,

$$R_{BB} = \frac{V_{CC} - V_{BE}}{I_B} = \frac{12 - 0.7}{3 \times 10^{-3}} \approx 3.9\,\text{k}\Omega.$$

7.3 CLASS B POWER AMPLIFIERS

Class B amplifiers are widely used because of the low standby DC current requirements, unlike Class A amplifiers that require an operating point characterized by a large collector current. The reduction in the standby or DC current requirement in Class B operation is achieved by biasing each of the two transistors at cut-off. This in turn reduces the quiescent collector power dissipation in the transistors.

Since Class B power amplifier operation has transistors conducting in only one half of the period of the input signal, two transistors are necessary in a *push-pull* arrangement to add the two halves of the cycle for the reconstruction of the entire amplified sinusoid, shown in Figure 7.20. The transformer load coupling shown in the Figure 7.7 is widely used. The collector supply is fed into the center tap of the output transformer primary. The base bias current is fed into the center tap of the input transformer secondary.

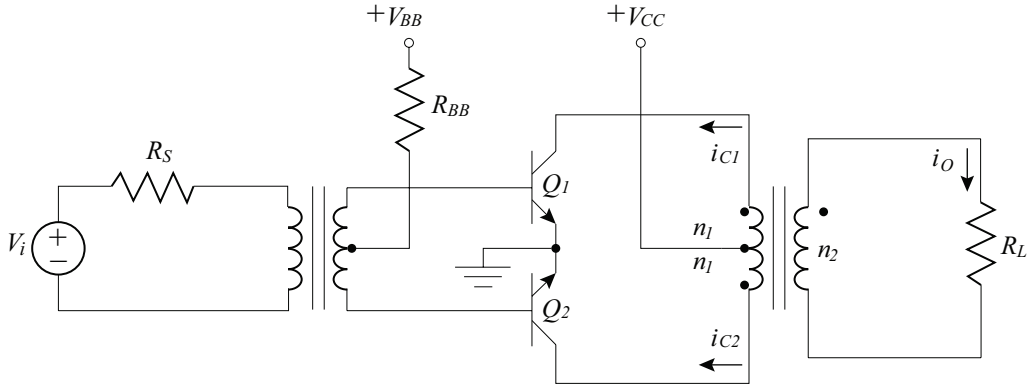


Figure 7.20: Class B common-emitter push-pull power amplifier.

A graphical construction for determining the output waveforms of a single Class B transistor stage (half of the push-pull stage) is shown in Figure 7.21.

A disadvantage of using Class B operation is the inherently nonlinear nature of the input characteristic of BJTs. This leads to distortion near the zero crossings of the output current i_O.

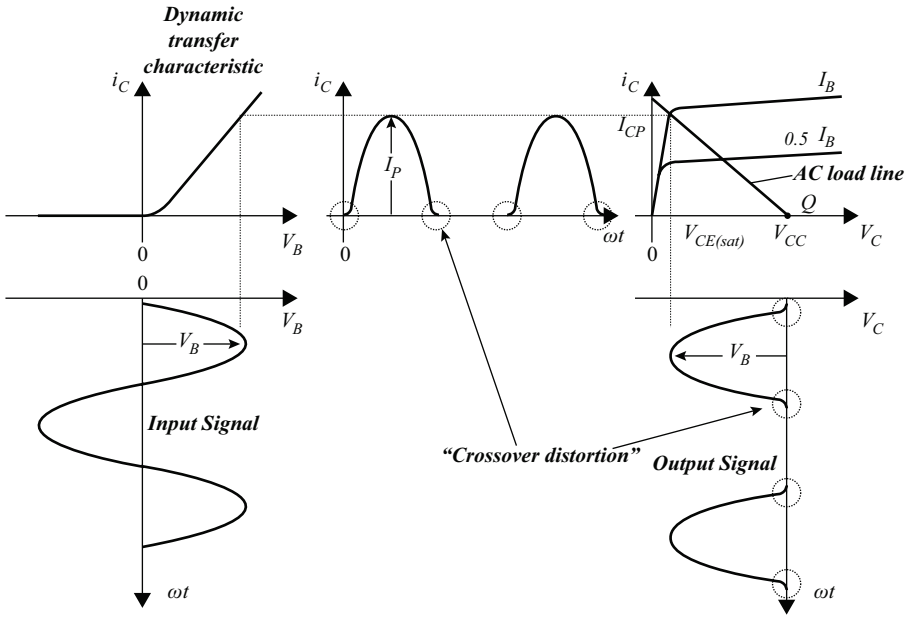


Figure 7.21: Waveforms of a single class B transistor stage (half of a push-pull stage) constructed with graphical methods.

The input characteristics and the resulting output in Figure 7.21 clearly shows the load current distortion. This distortion is referred to as the *crossover distortion*. Crossover distortion is best understood by studying Figure 7.22. The nonlinear input/output characteristic of the push-pull configuration is shown. The exponential nature of the curve indicates high input resistance at low signal levels. Little base current flows until the base-emitter voltage exceeds V_γ. The resulting collector current will also be small until the input voltage is sufficiently high since the I_C is essentially proportional to the base current. The resulting output from a push-pull Class B configuration is a sinusoid that exhibits crossover distortion.

It is customary to treat only one transistor when analyzing the push-pull configuration since each is operating at identical currents and voltages into an identical load, under the assumption that the transistors have identical characteristics. The output characteristic with load line of one of the transistors in the Class B amplifier of Figure 7.20 is shown in Figure 7.23.

The DC load line per transistor is one-half of the resistance of the output transformer primary. If high-quality output transformers are used, the resistance of the primary can be assumed to be negligible. Therefore, the DC load line has an infinite negative slope. The AC load line has a slope of $-1/R'_L$, where

$$R'_L = \left(\frac{n_1}{n_2}\right)^2 R_L. \tag{7.55}$$

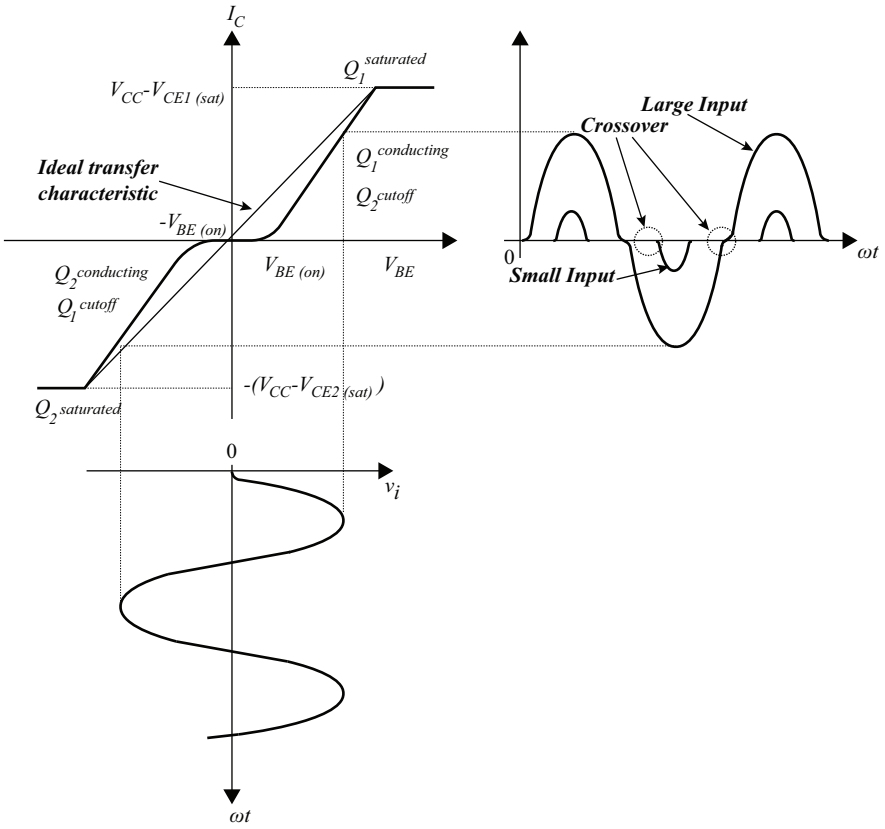


Figure 7.22: Output waveforms of a Class B amplifier for varying input signals.

R'_L is the AC load per transistor, n_1 is one-half the total number of primary turns on the output transformer, n_2 is the number of secondary turns on the output transformer, and R_L is the actual load.

To analyze the Class B push-pull configuration, it is assumed that each transistor is operating at identical levels driving identical loads. The DC load per stage consists of one-half of the total primary DC resistance which, for good transformers, can be considered to be negligible. Each collector circuit has only one-half of the total primary turns or n_1 turns (referred to Figure 7.20) for an AC resistance of R'_L per transistor or a total AC primary resistance of $4R'_L$.

In Figure 7.23, the load line indicates an operating point at $I_C = 0$ and $V_{CE} = V_{CC}$. A load line joins this point with $I_C = I_{CP}$ and $V_{CE} = 0.2\,\text{V}$. Then the AC resistance is,

$$R'_L = \frac{V_{CC} - V_{CE(sat)}}{I_{CP}} \approx \frac{V_{CC}}{I_{CP}}, \quad \text{for } V_{CC} \gg V_{CE(sat)}. \tag{7.56}$$

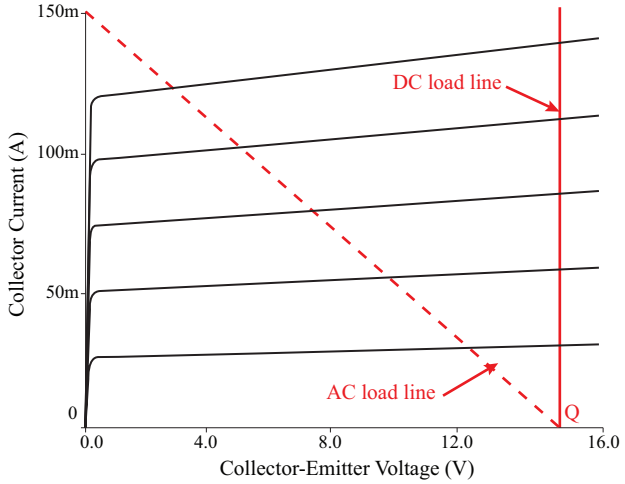


Figure 7.23: Output characteristic with load line of one of the transistors in the Class B amplifier of Figure 7.20.

The power delivered per transistoris to the load is,

$$P_{AC,per\ transistor} = \frac{1}{2}\left(\frac{V_{CC} - V_{CE(sat)}}{\sqrt{2}}\right)\left(\frac{I_{CP}}{\sqrt{2}}\right) \approx \frac{V_{CC} I_{CP}}{4}. \tag{7.57}$$

The factor of 1/2 is used because each transistor passes a half-wave signal. For the push-pull pair,

$$P_{AC} = \left(\frac{V_{CC} - V_{CE(sat)}}{\sqrt{2}}\right)\left(\frac{I_{CP}}{\sqrt{2}}\right) \approx \frac{V_{CC} I_{CP}}{2}. \tag{7.58}$$

The DC power delivered to the Class B push-pull amplifier is negligible during standby operation. When a sinusoid of peak amplitude I_{CP} is produced by the amplifier, each transistor conducts during one half of the period of the sinusoid,

$$I_{DC,Q1} = I_{DC,Q2} = \frac{1}{T}\int_0^{\frac{T}{2}} I_{CP} \sin \omega t \, dt. \tag{7.59}$$

Solving Equation (7.59) yields,

$$\begin{aligned} I_{DC,Q1} = I_{DC,Q2} &= \int_0^{\frac{T}{2}} I_{CP} \sin \omega t \, dt \\ &= \frac{\omega}{2\pi}\int_0^{\frac{\pi}{\omega}} I_{CP} \sin \omega t \, dt \\ &= \frac{I_{CP}}{\pi}. \end{aligned} \tag{7.60}$$

Therefore, the total current delivered by the power supply is,

$$I_{DC} = I_{DC,Q1} + I_{DC,Q2} = \frac{2I_{CP}}{\pi}. \tag{7.61}$$

Then the total power delivered by the power supply is,

$$P_{DC} = V_{CC} I_{DC} = \frac{2V_{CC} I_{CP}}{\pi}. \tag{7.62}$$

The maximum efficiency of the Class B push-pull power amplifier is found to be,

$$\eta_{\max} = \frac{P_{AC}}{P_{DC}} \times 100\% = \frac{\frac{V_{CC} I_{CP}}{2}}{\frac{2V_{CC} I_{CP}}{\pi}} \times 100\% = \frac{\pi}{4} \times 100\% \approx 78\%. \tag{7.63}$$

For Class B power amplifiers, η is linearly dependent on signal strength, while in Class A amplifiers, it is dependent on the square of the signal strength.

Should a Class B power amplifier be driven to a fraction of its total allowable swing,

$$\Delta V_C = k V_{C,\max} \quad \text{and} \quad \Delta I_C = k I_{C,\max}, \tag{7.64}$$

where k is a fraction of the otal allowable swing, and ΔV_C and ΔI_C are the actual voltage and current swings, respectively. Therefore, the actual full load power is,

$$P_{FL,actual} = \frac{(k V_{C,\max})(k I_{C,\max})}{4}. \tag{7.65}$$

Example 7.3

Design a 10 W servo amplifier to meet the following specifications:

Rated load power:	10 W
Load:	500 Ω (a small instrument motor)
Overload capacity:	10%
Input resistance:	50 kΩ minimum
Output transformer efficiency:	80%
Carrier frequency:	400 Hz
Power Supplies:	28 V.

Matched transistors are available: MJE15028 (*npn*) and MJE15029 (*pnp*).

Solution:

The circuit arrangement of Figure 7.20 will be used.

The full load power is $P_{FL} = 10\,W$. To supply P_{FL} to the load is,

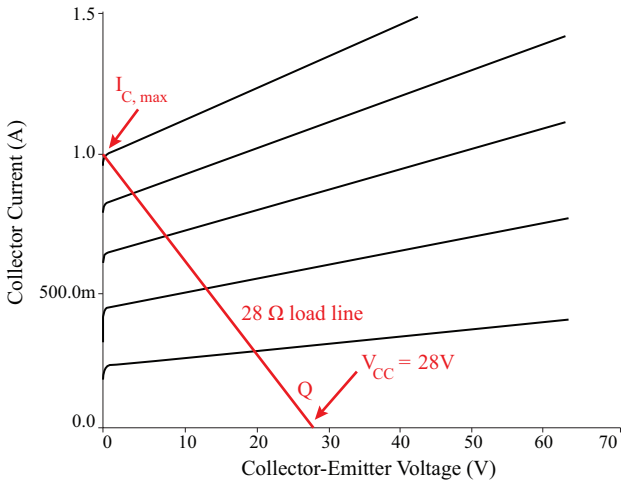
$$\text{Transformer Primary Power} = \frac{P_{FL}}{\eta_{xfmr}} = \frac{10}{0.8} = 12.5\ \text{W}.$$

For a 10% overload capacity, the power amplifier must be capable of handling

$$(110\%)(12.5) = 13.7\,\text{W}.$$

Therefore, each transistor in the Class B push-pull amplifier must supply

$$\frac{13.7\ \text{W}}{2} = 6.85\ \text{W}.$$



From the load line analysis shown,

$$V_{C,\max} = V_{CC} - V_{CE(sat)} \approx V_{CC} = 28\,\text{V}.$$

For each transistor under overload conditions,

$$P_{AC\ per\ transistor} = \frac{V_{C,\max} I_{C,\max}}{4}.$$

Solving for $I_{C,\max}$,

$$I_{C,\max} = \frac{4P_{AC\ per\ transistor}}{V_{C,\max}} = \frac{4(6.85)}{28} \approx 1.0\ \text{A}.$$

Therefore, the AC load that each transistor must drive is,

$$R'_L = \frac{V_{C,\max}}{I_{C,\max}} = \frac{28}{1} = 28\ \Omega,$$

(which is the negative reciprocal of the slope of the load line), and the total primary AC load resistance is

$$R'_L = 2^2(28) = 112\,\Omega.$$

The output transformer turns ratio is then

$$\frac{n_1}{n_2} = \sqrt{\frac{R'_L}{R_L}} = \sqrt{\frac{28}{500}} = 0.24.$$

The full load power for each transistor is,

$$P_{FL,per\ transistor} = \frac{P_{FL}}{2} = \frac{12.5}{2} = 6.25\ \text{W}.$$

The actual swings for the rated full load are found using the laws of similar triangles applied to the load line graph,

$$P_{FL,actual} = \frac{(\Delta I_C)(\Delta V_C)}{4} = \frac{(k I_{C,\max})(k V_{C,\max})}{4}.$$

This yields $k = 0.89$. Therefore, the maximum output swings are,

$$\Delta I_C = k I_{C,\max} \approx 0.9\ \text{A} \quad \text{and} \quad \Delta V_C = k V_{C,\max} \approx 25\ \text{V},$$

and the actual full load power is $(0.9)(25) = 5.6\,\text{W}$ per transistor or 11.2 W total.

7.3.1 COMPLEMENTARY CLASS B (PUSH-PULL) OUTPUT STAGE

A simplified version of a complementary Class B amplifier arrangement that is often used as an integrated circuit output stage is shown in Figure 7.24. This arrangement uses complementary transistors (one *pnp* and one *npn*) in common-collector configuration. By using complementary transistors, the need for input and output transformers is eliminated. The transfer characteristic is identical to that of the transformer coupled Class B power amplifier.

The principle of operation of the simplified complementary Class B output stage is as follows. For $|V_i| < V_{BE(on)}$, both Q_1 and Q_2 are cutoff. When $V_i > V_{BE(on)}$, Q_1 turns on and enters the forward saturation region. Q_2 remains in cutoff. The upper limit on V_o occurs when Q_1 saturates at $V_i = V_{CC} - V_{CE1(sat)}$. For negative values of V_i, the same situation holds true with when the roles of Q_1 and Q_2 are reversed. The lower limit on V_o occurs when Q_2 saturates at $V_i = -(V_{CC} - V_{CE2(sat)})$.

CMOS power buffers in the inverter configuration, as discussed in Chapter 4 (Book 1), are commonly used to interface CMOS logic to saturated logic (e.g., TTL). This practice is common in instances where a conventional CMOS gate may not be able to supply the required input power, while at the same time provide sufficiently low output voltages for the TTL gates.

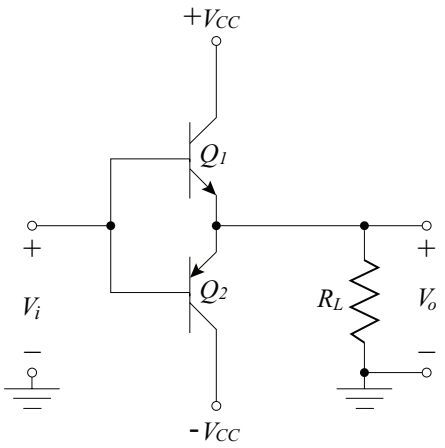


Figure 7.24: Simplified complementary Class B output stage.

It is common to use feedback to reduce or eliminate crossover distortion.[3] One arrangement that is used is to employ feedback with an unity gain OpAmp configuration shown in Figure 7.25.

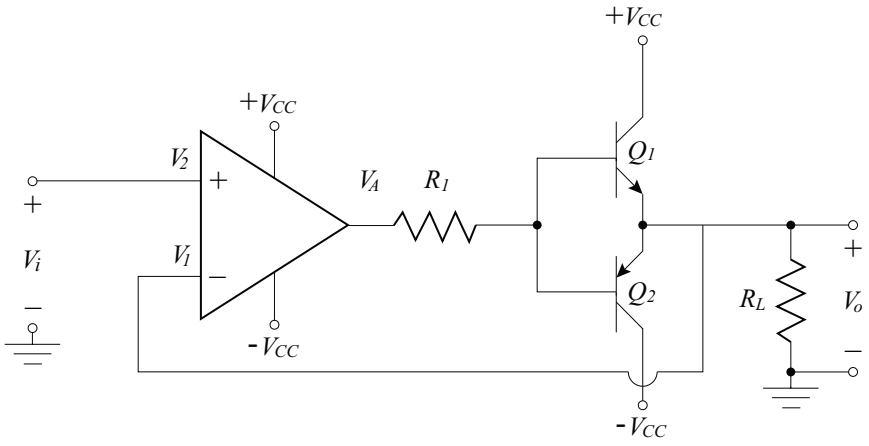


Figure 7.25: Use of feedback to eliminate crossover distortion in Class B amplifiers.

Define the open-loop gain of the OpAmp as A which is very large ($\approx 200\,\text{k}$). Then the output voltage from the OpAmp is,

$$V_A = A(V_2 - V_1). \tag{7.66}$$

[3]Chapter 8 provides a complete discussion of the use of the reduction of distortion due to feedback.

From Equation (7.66) when $V_A = V_{BE(on)} = 0.6\,\text{V}$,

$$\frac{V_A}{A} = \frac{0.6}{A} = V_2 - V_1. \tag{7.67}$$

Therefore, when $V_1 = 0$, then

$$V_2 = \frac{0.6}{A} = \frac{0.6}{200 \times 10^3} \ll 0.6\,\text{V}. \tag{7.68}$$

Equation (7.68) indicates that for a very small input at $V_2 = V_i$, the output voltage from the push-pull stage is zero. Therefore, the crossover region in the transfer characteristic has been reduced from $\pm V_{BE(on)}$ to less than $5\,\mu\text{V}$. So essentially, there is no crossover distortion to speak of when using the configuration in Figure 7.25.

7.4 CLASS AB POWER AMPLIFIERS

In Section 7.3, Class B power amplifiers were shown to have a maximum efficiency of approximately 78.5%. Unfortunately, feedback was required to eliminate the nonlinear transfer characteristic caused by crossover distortion.

An alternate method to feedback for reducing or nearly eliminating crossover distortion is to bias each transistor in the push-pull configuration so that they are barely in the forward active region with $V_i = 0$. One possible configuration to achieve this bias condition to eliminate crossover distortion is shown in Figure 7.26. This class of amplifier is called a Class AB power amplifier/output stage since the transistors are always biased as in Class A operation, but is biased at a fraction of the peak load current as in Class B operation.

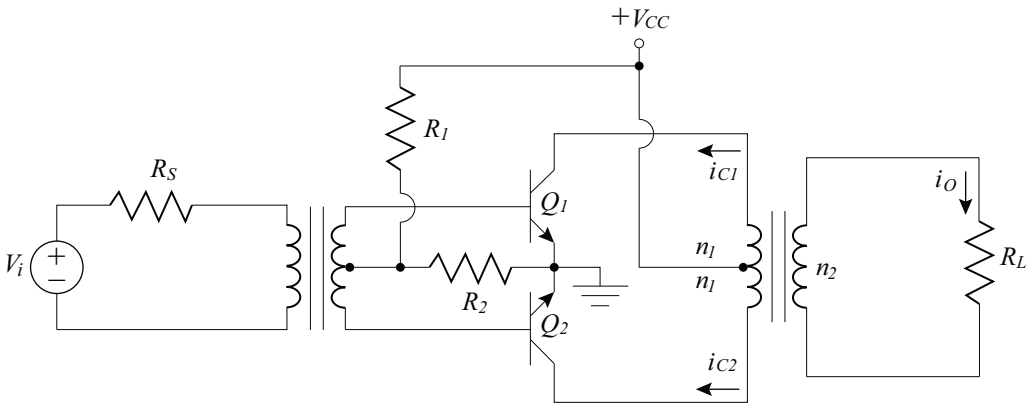


Figure 7.26: Class AB power amplifier configuration.

In Figure 7.26, the resistors R_1 and R_2 are adjusted to that the transistors Q_1 and Q_2 are just barely forward biased, or $V_{BQ1} = V_{BQ2} = V_{BE(on)}$ for matched transistors. The operation of the circuit in Figure 7.26 is as follows:

Both Q_1 and Q_2 are biased so that the base-emitter voltage of each transistor is $V_{BE(on)}$ for $V_i = 0$. For an input to Q_1 of less than V_i, the transistor is cutoff. For $V_i \geq V_{BE(on)}$, Q_1 turns on and is in the forward active region. The output voltage due to Q_1 saturates at $V_{CC} - V_{CE1(sat)}$. Conversely for Q_2, if $V_i > V_{BE(on)}$ the transistor is cutoff. Q_2 turns on when $V_i \leq V_{BE(on)}$. The output voltage due to Q_2 saturates at $-(V_{CC} - V_{CE2(sat)})$. The transfer characteristic is shown in Figure 7.27. The characteristic curve for each transistor is shown as well as the resulting composite transfer characteristic. The composite transfer characteristic is found by adding the transfer characteristics of the two transistors. The resulting composite transfer characteristic shows no crossover distortion.

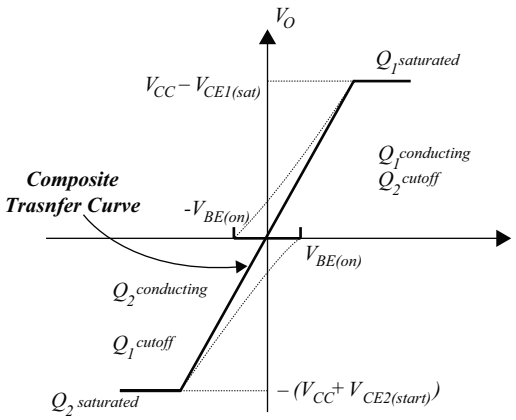


Figure 7.27: The transfer characteristic of the Class AB power amplifier shown in Figure 7.26.

An integrated circuit implementation of a Class AB output stage is shown in Figure 7.28a. The Class AB output stage shown is used in the μA741 OpAmp. A simplified version of the μA741 output stage is shown in Figure 7.28b.

In analyzing Figure 7.28b, Q_{13A} acts as a constant current source of 0.22 mA. Q_{23} is the input transistor to the Class AB output stage. With $V_i = 0$, the output complementary transistor pair Q_{14} and Q_{20} are biased at a collector current of about 0.17 mA by the diodes Q_{19} and Q_{18}. The current through Q_{19} and Q_{18} produces a voltage,

$$V_{BE19} + V_{BE18} = V_{BE14} + V_{EB20}. \tag{7.69}$$

As V_i goes negative, the base of Q_{20} and V_O follows (since Q_{23} and Q_{20} are in common-collector configurations), with Q_{20} drawing current from R_L. When V_i is $-V_{CC}$, the output voltage is limited to

$$V_{O(neg)} = -V_{CC} - V_{BE23} - V_{BE20}. \tag{7.70}$$

The negative voltage limit is about $0.7\,\text{V} + 0.7\,\text{V} = 1.4\,\text{V}$ more positive than the negative rail voltage ($-V_{CC}$).

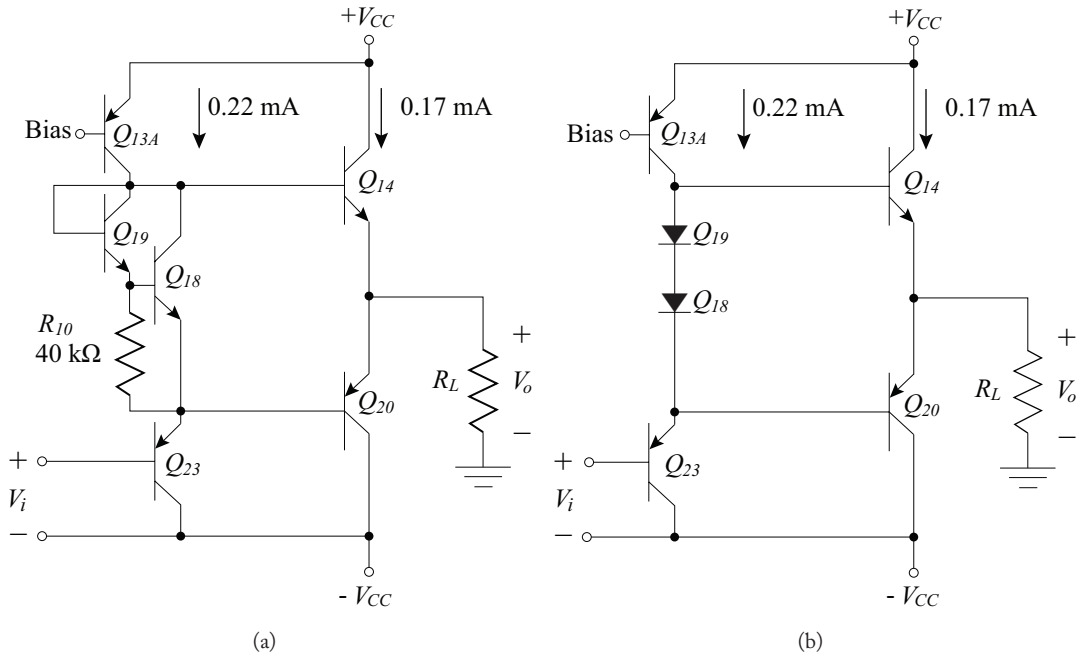


Figure 7.28: μA741 OpAmp output stage (a) Actual schematic; (b) Simplified schematic.

As V_i increases in the positive direction from $V_i = 0$, the output voltage and the base of Q_{20} follows with Q_{14} delivering the current to the load. When V_i is $+V_{CC}$, the output voltage is limited by $Q_{13\,\mathrm{A}}$ saturating. The positive limit of the output voltage is,

$$V_{O(pos)} = V_{CC} - V_{CE13\,\mathrm{A}(sat)} - V_{BE14}. \tag{7.71}$$

The positive voltage limit is approximately $0.7\,\mathrm{V} + 0.2\,\mathrm{V} = 0.9\,\mathrm{V}$ less than the positive voltage rail (V_{CC}).

The conversion efficiency of a Class AB amplifier is somewhat less that that of a Class B amplifier. This reduction in efficiency is due to an additional term in the DC power due to the quiescent current necessary to achieve minimal crossover distortion:

$$P_{DC} = \frac{2V_{CC}I_{CP}}{\pi} + V_{CC}I_{Bias}. \tag{7.72}$$

Therefore, the maximum efficiency fora Class AB amplifier is given by:

$$\eta_{\max} = \frac{\dfrac{V_{CC}I_{CP}}{2}}{\dfrac{2V_{CC}I_{CP}}{\pi} + V_{CC}I_{Bias}} \times 100\% = \frac{\pi I_{CP}}{4I_{CP} + 2\pi I_{Bias}} \times 100\%. \tag{7.73}$$

It is interesting to compare the efficiency of well-designed amplifiers as a function of output signal strength (Figure 7.29). The output power of all amplifiers is proportional to the square of output signal strength. Class A amplifiers are characterized by constant DC power: this results in a parabolic efficiency curve. Class B amplifiers are characterized by DC power that is proportional to signal strength: a linear efficiency curve results. Class AB amplifiers lie between the two other classes with Class B as an upper limit.

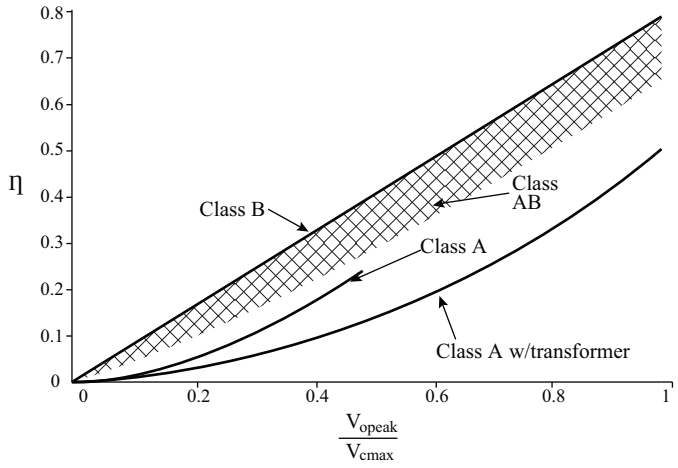


Figure 7.29: Typical conversion efficiency of well-designed power amplifiers as a function of output signal amplitude.

In order to increase the gain of output stages in integrated circuits while reducing base currents, compound transistors in dual common-collector Darlington pairs are commonly used (see Section 6.2.1). Compound *pnp* Darlington configurations are also used. Since in good quality *pnp* BJTs are difficult to fabricate in integrated circuits, an alternate compound configuration shown in Figure 7.30 is often used. This compound transistor has a current gain of $\beta \approx \beta_1 \beta_2$.

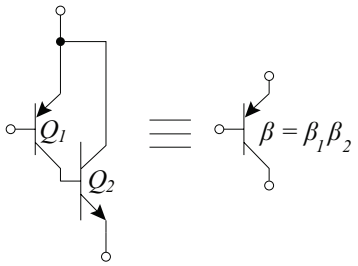


Figure 7.30: Compound *pnp* BJT.

7.5 DISTORTION

When the output signal waveform of an amplifier differs in general shape from the input signal waveform, the output is said to be distorted. In particular, if a single-frequency input to an amplifier results in an output composed of the input frequency and other frequencies, the amplifier has distorted the signal. The creation of additional frequencies is typically the result of non-linear distortion.

Earlier, it was shown that large input signals to amplifiers caused the amplifier under test to yield distorted output signals. In this section, a systematic description of distortion is developed. With this description, two common industry definitions of distortion are developed and related to each other.

An incrementally linear power amplifier[4] has a transfer characteristic described by

$$v_O = V_{DC} + a_1 v_i, \tag{7.74}$$

where

$v_O \equiv$ the output voltage,
$v_i \equiv$ the input voltage (AC and DC components possible),
$a_1 \equiv$ the voltage gain,
$V_{DC} \equiv$ the DC offset voltage at the output.

The principle of superposition applies to incrementally linear systems in a unique manner. That is, if

$$v_{O1} = V_{DC} + a_1 v_{i1} \quad \text{and} \quad v_{O2} = V_{DC} + a_1 v_{i2}, \tag{7.75}$$

then the total output of a incrementally linear system is,

$$v_O = V_{DC} + a_1 (v_{i1} + v_{i2}). \tag{7.76}$$

In electronic amplifiers, the DC component, V_{DC}, consists of the bias or quiescent point of the circuit.

Superposition no longer applies when the transfer characteristic is non-linear. Figure 7.31 shows a transfer characteristic of a power amplifier.
The region in Figure 7.31 that is not clipped is described by the power series,

$$v_O = V_{DC} + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \cdots . \tag{7.77}$$

For a sinusoidal input, $v_i = X \cos \omega t$, the power series in Equation (7.77) is,

$$v_O = V_{DC} + a_1 X \cos \omega t + a_2 (X \cos \omega t)^2 + a_3 (X \cos \omega t)^3 + \cdots . \tag{7.78}$$

[4]Incremental linearity was previously discussed in Chapter 5.

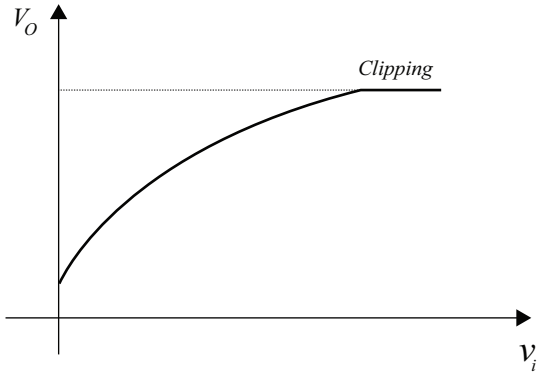


Figure 7.31: Non-linear transfer characteristic of a power amplifier.

Using trigonometric identities, Equation (7.78) is,

$$v_O = \left(V_{DC} + \frac{a_2 X^2}{2}\right) + \left(a_1 X + \frac{3a_3 X^3}{4}\right)\cos\omega t + \left(\frac{a_2 X^2}{2}\right)\cos 2\omega t + \left(\frac{a_3 X^3}{4}\right)\cos 3\omega t + \cdots \tag{7.79}$$

where the fourth and higher harmonics may be ignored with negligible error.[5] Inspection of Equation (7.79) shows that harmonics are generated by the non-linear transfer characteristic. Harmonics are sinusoidal terms that are multiples of the fundamental frequency, ω, that is the same frequency as the input signal. For linear power amplifiers, the presence of harmonics is undesirable and are the direct result of non-linear distortion.

Additionally, there is a shift in the DC or quiescent point by the addition of a term containing the constant for the squared term in the power series. The fundamental ($\cos\omega t$) term also has increased beyond the amplification constant associated with the fundamental by a term proportional to the constant for the cubed term in the power series.

Equation (7.79) can be represented by a Fourier Series,

$$v_O = V_{DC} + A_0 + A_1\cos\omega t + A_2\cos 2\omega t + A_3\cos 3\omega t + \cdots, \tag{7.80}$$

where A_0, A_1, A_2, and A_3 are the Fourier coefficients. One method that may be used to determine the Fourier coefficients is a method due to Espley.[6] A pure sinusoidal signal voltage is applied to the input of the power amplifier. The input and output waveforms are sampled at several times intervals to obtain the Fourier coefficients of Equation (7.80). To evaluate the four coefficients

[5]This approximation is valid in typical amplifiers where distortion is relatively small. In cases of extremely large distortion, higher-order terms must be considered.

[6]Espley, D.C., The Calculation of Harmonic Production in Thermionic Valves with Resistive Loads, *Proc. IRE*, vol. 21, pp. 1439–1446, October, 1933.

in Equation (7.80), the values of the output at the four input voltages are determined as shown in Figure 7.32. For this example, the samples are taken at $\omega t = 0°, 60°, 120°$, and $180°$. with the corresponding output voltage is designated as $V_{0°}, V_{60°}, V_{120°}, V_{180°}$. The value at $\omega t = 90°$ is V_{DC} (the quiescent point). As noted earlier, the DC or quiescent point of the output has shifted away from the average value of the signal.

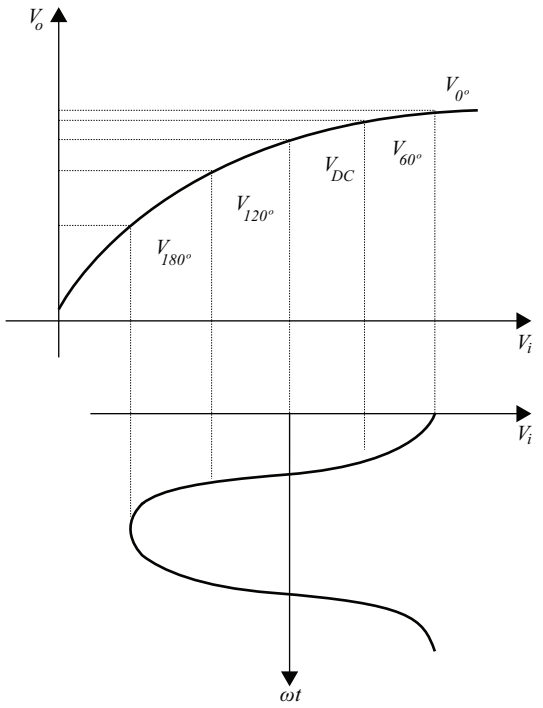


Figure 7.32: Graphical determination of the distortion content in the output voltage.

The values of the Fourier coefficients A_0, A_1, A_2 and A_3 in Equation (7.80) can theoretically be determined by substituting the values of the angle (ωt) into Equation (7.80) and solving the four simultaneous equations. That is,

$$\begin{aligned}
\omega t = 0° : &\quad V_{\max} = V_{DC} + A_0 + A_1 + A_2 + A_3, \\
\omega t = 60° : &\quad V_{60} = V_{DC} + A_0 + \frac{A_1}{2} - \frac{A_2}{2} - A_3, \\
\omega t = 120° : &\quad V_{120} = V_{DC} + A_0 - \frac{A_1}{2} - \frac{A_2}{2} + A_3, \\
\omega t = 180° : &\quad V_{\min} = V_{DC} + A_0 - A_1 + A_2 - A_3.
\end{aligned} \tag{7.81}$$

The solution to the four simultaneous equations in Equation (7.81) yields the expressions for the Fourier coefficients in Equation (7.80),

$$\begin{aligned} A_0 &= \frac{1}{6}\left(V_{0^\circ} + V_{180^\circ}\right) + \frac{1}{3}\left(V_{60^\circ} + V_{120^\circ}\right) - V_{DC}, \\ A_1 &= \frac{1}{3}\left(V_{0^\circ} - V_{180^\circ}\right) + \frac{1}{3}\left(V_{60^\circ} - V_{120^\circ}\right), \\ A_2 &= \frac{1}{3}\left(V_{0^\circ} + V_{180^\circ}\right) - \frac{1}{3}\left(V_{60^\circ} + V_{120^\circ}\right), \\ A_3 &= \frac{1}{6}\left(V_{0^\circ} - V_{180^\circ}\right) - \frac{1}{3}\left(V_{60^\circ} - V_{120^\circ}\right). \end{aligned} \tag{7.82}$$

The harmonic distortion is define as,

$$D_2 \equiv \frac{|A_2|}{|A_1|} \quad \text{and} \quad D_3 \equiv \frac{|A_3|}{|A_1|}, \tag{7.83}$$

and is commonly given as a percentage or in decibels where D_2 is the second harmonic distortion and D_3 is the third harmonic distortion. In terms of decibels, the second and third harmonic distortions are

$$D_2[dB] \equiv 20\log\frac{|A_2|}{|A_1|} \quad \text{and} \quad D_3[dB] \equiv 20\log\frac{|A_3|}{|A_1|}, \tag{7.84}$$

and are negative numbers indicating that the voltage amplitude of the harmonic components is less than the fundamental. The total harmonic distortion (THD) is commonly given as a percentage and is expressed as the ratio of the rms values of all the harmonic terms to the effective value of the fundamental, and is used extensively in audio amplifier specifications,

$$\text{THD} = \frac{\sqrt{A_2^2 + A_3^2 + \cdots}}{|A_1|} \times 100\% = \sqrt{D_2^2 + D_3^2 + \cdots} \times 100\%. \tag{7.85}$$

If the distortion is not negligible, the total power delivered at the output load R_L is,

$$\begin{aligned} P_O &= \frac{\left(A_1^2 + A_2^2 + A_3^2 + \cdots\right)}{2R_L} \\ &= \left\{1 + \left[A_1\left(\frac{\text{THD}}{100}\right)\right]^2\right\} P_1, \end{aligned} \tag{7.86}$$

where the fundamental power is

$$P_1 = \frac{A_1^2}{2R_L}. \tag{7.87}$$

As an example, state-of-the-art audio power amplifiers that incorporate negative feedback to compensate for non-linearlity typically have THD of less than 0.003% at low frequencies and low

output power levels.[7] In cable television applications, the radio frequency (RF) power amplifiers also require very low distortion levels to deliver acceptable picture quality.

Because the distortion levels are so low, the method of Espley using the direct measure of the transfer characteristic yields inaccurate distortion data due to noise and other spurious factors. Instead, it is common practice to test amplifier non-linearlity directly by using a pure sinusoidal input. At the output, the harmonics are measured directly using a spectrum analyzer which displays the rms magnitude (or power) of the frequency components of the output signal. The fundamental and harmonics appear on the CRT of the spectrum analyzer as spikes. Measurement of the peak of the harmonic spikes relative to the fundamental spike yields the amplifier THD. Other analyzers (e.g., audio analyzers) perform the above operation automatically and display the THD on its front panel.

Another method, commonly used in RF and microwave electronics, for finding the amount of distortion of an amplifier is the two-tone ratio (TTR) method for determining harmonic and intermodulation distortion (IMD) products. In the TTR method, two signals with identical amplitudes that are separated by some frequency are combined and used as the input to the amplifier. The output frequency components are then analyzed for distortion.

Consider the non-linear transfer function of Equation (7.77) rewritten here for convenience,

$$v_O = V_{DC} + a_1 v_i + a_2 v_i^2 + a_3 v_i^3 + \cdots .$$

Two sinusoids are added so that the input signal is,

$$v_i = X_1 \cos \omega_1 t + X_2 \cos \omega_2 t. \tag{7.88}$$

Substituting Equation (7.88) into Equation (7.77) yields,

$$\begin{aligned} v_O = {} & V_{DC} + a_1 \left(X_1 \cos \omega_1 t + X_2 \cos \omega_2 t\right) + a_2 \left(X_1 \cos \omega_1 t + X_2 \cos \omega_2 t\right)^2 \\ & + a_3 \left(X_1 \cos \omega_1 t + X_2 \cos \omega_2 t\right)^3 + \cdots . \end{aligned} \tag{7.89}$$

By using trigonometric identities, Equation (7.89) is put in a form similar to Equation (7.79) to yield the magnitude and frequency components of the output signal,

$$v_o = \left[V_{DC} + \frac{1}{2} a_2 \left(X_1 + X_2\right)\right] \qquad \text{(DC term)}$$

[7]Negative feedback is discussed in Chapters 8 and 11 (Book 3).

$$
\begin{aligned}
&\left.\begin{aligned}&+\left[a_1X_1+\tfrac{3}{2}a_2\left(X_1X_2^2+\tfrac{1}{2}X_1^3\right)\right]\cos\omega_1 t\\&+\left[a_1X_2+\tfrac{3}{2}a_3\left(X_2X_1^2+\tfrac{1}{2}X_2^3\right)\right]\cos\omega_2 t\end{aligned}\right\} && \text{(fundamentals)}\\
&+\frac{1}{2}a_2\left(X_1^2\cos 2\omega_1 t+X_2^2\cos 2\omega_2 t\right) && (2^{\text{nd}}\text{ harmonics})\\
&+a_2X_1X_2\left[\cos\left(\omega_1-\omega_2\right)t+\cos\left(\omega_1+\omega_2\right)t\right] && 2^{\text{nd}}\text{-order IMD products}\\
&+\frac{1}{4}a_3\left(X_1^3\cos 3\omega_1 t+X_2^3\cos 3\omega_2 t\right) && 3^{\text{rd}}\text{ harmonics}\\
&\left.\begin{aligned}&+\tfrac{3}{4}a_3X_1^2X_2\left[\cos\left(2\omega_1-\omega_2\right)t+\cos\left(2\omega_1+\omega_2\right)t\right]\\&+\tfrac{3}{4}a_3X_1X_2^2\left[\cos\left(2\omega_2-\omega_1\right)t+\cos\left(2\omega_2+\omega_1\right)t\right]\end{aligned}\right\} && 3^{\text{rd}}\text{-order IMD products.}
\end{aligned}
\tag{7.90}
$$

In the TTR method, new sum and difference frequencies of the two input frequencies are created and are called intermodulation (IMD) products or sometimes "beat" frequencies. The new sum and difference frequencies are not harmonically related to either of the two fundamental input frequencies.

There are several reasons for using the TTR method over single frequency harmonic measurement methods. They include:

- Difficulty in generating a pure sinusoid. All real signal generators have some harmonic content.
- In single octave[8] systems (those systems that only operate in one octave) with multiple sinusoids closely spaced in frequency within the single octave, third order IMD products are of interest.

The relationship between the results of the TTR results and the harmonic coefficients for the Fourier series in Equation (7.80) can be found. The combination of the equal amplitude TTR input signals are adjusted to equal the total input power of a single sinusoid for the harmonic measurement. This relationship implies that the rms power of the two combined sinusoids for the TTR is equal to the rms value of the single input for the harmonic measurement,

$$X^2=\left(\frac{X_1}{\sqrt{2}}\right)^2+\left(\frac{X_2}{\sqrt{2}}\right)^2, \tag{7.91}$$

where X_1 and X_2 are the TTR inputs, and X is the input for the single frequency harmonic measurement.

For equal amplitude TTR inputs, $X_1=X_2$ so,

$$X_1=X_2=\frac{X}{\sqrt{2}}. \tag{7.92}$$

[8]An octave consists of a range of frequencies spanned by a factor of two.

Using Equation (7.92), the following relationships are found:

$$\begin{aligned}
\frac{\text{fundamental two tone}}{\text{fundamental single tone}} &= \frac{1}{\sqrt{2}}, \\
\frac{2^{\text{nd}}\text{harmonic two tone}}{2^{\text{nd}}\text{harmonic single tone}} &= \frac{1}{2}, \\
\frac{2^{\text{nd}}\text{IMD}}{2^{\text{nd}}\text{harmonic single tone}} &= 1, \\
\frac{3^{\text{rd}}\text{harmonic two tone}}{3^{\text{rd}}\text{harmonic single tone}} &= \frac{1}{2\sqrt{2}}, \\
\frac{3^{\text{rd}}\text{IMD}}{3^{\text{rd}}\text{harmonic single tone}} &= \frac{3}{2\sqrt{2}}.
\end{aligned} \tag{7.93}$$

Therefore, given TTR measure results, the Fourier coefficients in Equation (7.80) and the constants in the power series in Equation (7.77) can be found by applying Equation (7.93).

In Figure 7.31, as the output voltage starts to clip, another form of distortion takes place. This type of distortion is called *gain compression* and is due to a gradual decrease in the voltage gain of the amplifier which, in simple terms, reduces the gain coefficient to the fundamental signal in the Fourier series in Equation (7.77). This has the effect of increasing the ratio of the non-linear distortion products to the fundamental.

The push-pull arrangement of the Class B power amplifier (shown again in Figure 7.33) not only increases efficiency, but despite the effects of crossover distortion, has unique distortion canceling properties.

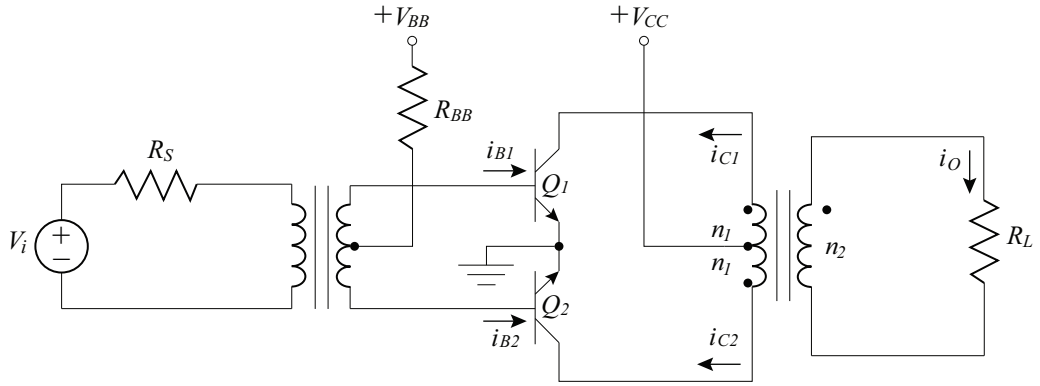


Figure 7.33: Class B push-pull arrangement.

Consider the base current in Q_1,

$$i_{B1} = I_{B(\max)} \cos \omega t. \tag{7.94}$$

The resulting Q_1 collector current can be expressed as a Fourier series,

$$i_{C1} = I_{CQ1} + A_0 + A_1 \cos \omega t + A_2 \cos 2\omega t + A_3 \cos 3\omega t + \cdots . \tag{7.95}$$

The corresponding base current in Q_2 is,

$$i_{B2} = -i_{B1} = I_{B(\max)} \cos(\omega t + \pi) . \tag{7.96}$$

Equation (7.96) implies that,

$$i_{B2}(\omega t) = i_{B1}(\omega t + \pi) . \tag{7.97}$$

Therefore, the Q_2 collector current is,

$$i_{C2} = I_{CQ2} + A_0 + A_1 \cos(\omega t + \pi) + A_2 \cos 2(\omega t + \pi) + A_3 \cos 3(\omega t + \pi) + \cdots . \tag{7.98}$$

Simplifying Equation (7.98) yields,

$$i_{C2} = I_{CQ2} + A_0 - A_1 \cos \omega t + A_2 \cos 2\omega t - A_3 \cos 3\omega t + \cdots . \tag{7.99}$$

Since the collector currents of Q_1 and Q_2 are in opposite directions through the output transformer primary, the total output current is proportional to the difference in collector currents,

$$\begin{aligned} i_{xfmr} &= k(i_{C1} - i_{C2}) \\ &= 2k(A_1 \cos \omega t + A_3 \cos 3\omega t + \cdots) , \end{aligned} \tag{7.100}$$

where k is a proportionality factor.

Equation (7.100) shows that there are only odd harmonics in the output signal when matched transistors are used. Even harmonics have been canceled out.

Because no even harmonics are present in the output of a push-pull amplifier, such a circuit will give more output per active device for a given amount of THD.

SPICE performs Fourier analysis on any waveform in a transient analysis using the Fourier command,

.FOUR <frequency value> <output variable>

The .FOUR command computes the amplitude and phase of any waveform with respect to frequency. The Fourier components may then be plotted.

SPICE can also calculated the intermodulation distortion components of a waveform using the command,

.DISTO <RLname> <number of points> <fstart> <fstop> <reference power>

7.6 THERMAL CONSIDERATIONS

The removal of heat from the BJT collector-base junction or the FET channel warrants considerable attention in power transistors due to the high power delivered to the load. For power BJTs,[9] metallic heat sinks are often necessary to remove the heat to the surrounding air. When possible, the metallic portion of the transistor case should make contact with the heat sink. However, it is common practice to use a mica washer as electrical insulation between the case and the heat sink. The washer is used to electrically isolate the heat sink from the case because in some power BJT packages, the collector is directly attached to the case.

A specification for the maximum allowable collector-junction temperature is found in the manufacturer's transistor specifications. This temperature is usually 150°C for silicon devices. Exceeding this temperature may cause irreparable damage to the transistor. The operating junction temperature, T_j, is dependent on the ambient temperature, T_a (typically 25°C), the thermal resistance, θ_T, of the heat transfer path from the junction to the surrounding and the power dissipated, P_D. This relationship is expressed as:

$$T_j = T_a + \theta_T P_D \quad \text{in °C.} \tag{7.101}$$

The total thermal resistance, θ_T has the units of Celsius/Watt.

The power dissipated by the transistor is almost entirely at the collector junction. Therefore, the power dissipated is,

$$P_D = V_{CE} I_C. \tag{7.102}$$

The maximum power dissipation is described by the maximum dissipation hyperbola and is,

$$P_{D(\max)} = (V_{CE} I_C)_{\max} = \frac{(T_{j(\max)} - T_a)}{\theta_T}. \tag{7.103}$$

The total thermal resistance is found by solving the heat transfer network analogous to an electrical network shown in Figure 7.34.

The current source represents the heat generated (or power dissipated by the BJT), and the three resistances represent the thermal resistances of the junction to case (θ_{jc}), case to heat sink (θ_{cs}), and heat sink to the ambient environment (θ_{sa}). The total thermal resistance is,

$$\theta_T = \theta_{jc} + \theta_{cs} + \theta_{sa} = \theta_{ja}. \tag{7.104}$$

For power transistors, the values of θ_{jc} is typically about 10°C/W. If the transistor case and the heat sink are insulated by a mica washer, θ_{cs} has values of around 0.5°C/W. The primary mode of heat removal from a power transistor is conduction by the heat sink and convection from the heat sink to the ambient surroundings. By blowing air over the heat sink, more heat may be removed.

[9]The discussion that follows is equally applicable to FETs.

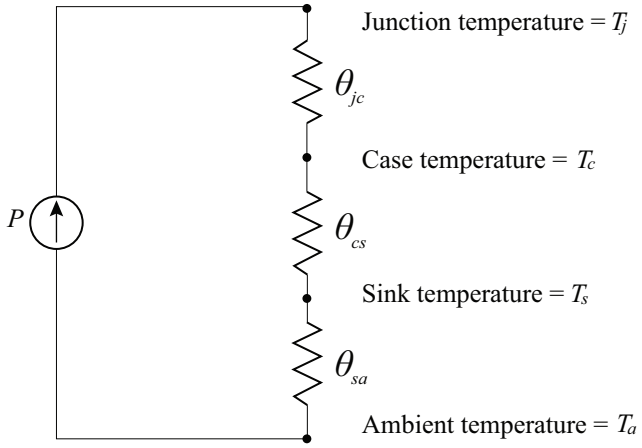


Figure 7.34: Heat transfer model.

Casual inspection of Equation (7.104) indicates that by removing the heat sink in the thermal path, the limitation on the power handling capacity is eliminated. However, by doing so, the case to ambient convection and radiation has significantly higher thermal resistance thereby reducing the ability of the device to dissipate heat: power handling capacity is actually diminished for this case.

Not shown in Figure 7.34 are associated thermal capacitances in parallel with each resistance. The capacitance is used to model transient thermal behaviour. The thermal time constant (resistance times capacitance) is long for the external components of the thermal model, but short for the transistor itself.

Thermal runaway can result if the rate of increase in the power dissipation with junction temperature exceeds the ability of the heat transfer network to remove the heat. The dissipated heat energy removed by the networks is found by differentiating Equation (7.101) with respect to T_j. The necessary condition for thermal stability is,

$$\frac{\partial V_{CE} I_C}{\partial T_j} < \frac{1}{\theta_T}. \tag{7.105}$$

For a constant collector-emitter voltage, the stability condition is,

$$V_{CE} \frac{\partial I_C}{\partial T_j} < \frac{1}{\theta_T}. \tag{7.106}$$

Variations in the current amplification factor and in the leakage current of the transistor causes the change in collector current with temperature, and is ultimately dependent on the bias circuitry.

With leakage current suspected of being the chief contributor to the collector current excursions,

$$V_{CE}\left(\frac{\partial I_C}{\partial I_{CO}}\right)\left(\frac{\partial I_{CO}}{\partial T_j}\right)_{\max} < \frac{1}{\theta_T}. \tag{7.107}$$

But from Section 3.7 (Book 1), the stability factor

$$S_I = \frac{\partial I_C}{\partial I_{CO}}. \tag{7.108}$$

For a thermally stable network, Equation (7.107) is rewritten as,

$$\left(\frac{\partial I_{CO}}{\partial T_j}\right)_{\max} < \frac{1}{\theta_T V_{CE} S_I}. \tag{7.109}$$

Despite using stable bias arrangements and effective heat transfer configurations, the transistor case temperature cannot be held at ambient temperature. Therefore, manufacturers provide a power-temperature derating curve (shown in Figure 7.35).

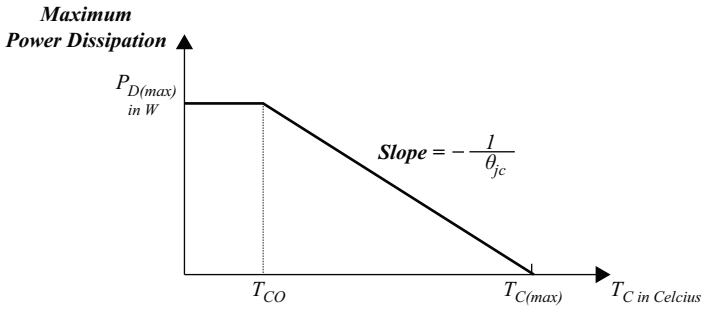


Figure 7.35: Transistor power dissipation derating curve.

In Figure 7.35, T_{CO} is the temperature where the derating begins. The maximum safe power dissipation, as specified by the manufacturer, is achieved when $T_C = T_{C(\max)}$. The curve of the same form as in Figure 7.35 can be used to find the power dissipation as a function of the junction temperature T_j, where T_j is the abscissa.

Example 7.4

For a case temperature of 120°C for a 50 W power transistor rated at 35°C, find the maximum power dissipated. The slope of the derating curve is 0.55 W/°C.

Solution

$$P_{D(\max)} = 50\,\text{W at } 35°\text{C}.$$

Using the equation of a line the power dissipated at 120°C can be found,

$$(120°\text{C} - 35°\text{C})(0.55\,\text{W}/°\text{C}) = 46.75\,\text{W}.$$

Therefore, the device power dissipation at 120°C is,

$$P_D = (50\,\text{W} - 46.75\,\text{W}) = 3.25\,\text{W at } 120°\text{C}.$$

7.7 CONCLUDING REMARKS

Different classes of amplifiers designed for the transfer of high power to loads were analyzed. The analysis of the amplifiers required the use of large-signal analysis methods. Because of the large signal excursions, the output waveforms experience distortion.

The most commonly used power amplifier/output stage classifications are the Class A, B, and AB. In Class A operation, the transistor conducts over the whole period (360°) of the input signal. In Class B operation, each of the two transistors conducts over half the period (180°). In Class AB operation, each transistor conducts over a time greater than half the period.

Since high powers may be delivered by these circuits, the conversion of DC power to signal power must be efficient. The theoretical maximum efficiencies for the different Classes of amplifiers are: 25% for Class A, 50% for Class A output transformer coupled amplifiers, 78.5% for Class B, and less than 78.5% for Class AB operation.

Distortion analysis was presented with a comparison between the Total Harmonic Distortion and Two-Tone Ratio methods of measurement.

Since power amplifiers deliver high power to their loads, the transistor may dissipate large amounts of power in the form of heat. Therefore, a heat transfer model was analyzed and related to the stability factor.

Summary Design Example: Public Address (PA) System Amplifier

In most audio electronic systems, the object is to drive one or more speakers. Typically, these speakers can be modelled as 8 Ω devices. Therefore, the output stage of audio electronic systems require the ability to provide maximum power transfer to a very low resistance device. One common method to drive low resistance devices is through the use of an output transformer. The purpose of the output transformer is to provide for impedance matching between the active devices and the speaker.

The output stage of a PA system will require the application of an electronic signal to an 8 Ω speaker. Although PA systems generally do not require high audio fidelity, a low distortion system is desired since some music may be amplified on the system. For a low to moderate power PA system, the rated (or full) load power can be in the order of 25 W, with an overload capacity of 10%. A single rail +24 V volt power supply is commonly used. The output resistance of the circuit that drives the output stage is 600 Ω.

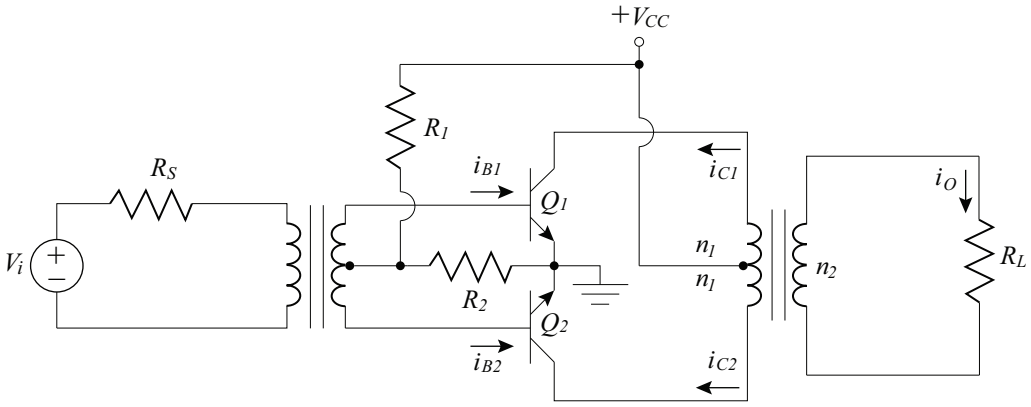
Design an output power amplifier stage to fulfill the requirements given.

Solution:

Several alternate output power stages topologies can be used in the design. These include:

- Class A
- Class B
- Class AB

A transformer-coupled Class AB power amplifier topology, shown below, is chosen because of its low distortion characteristic, and since power dissipation is not specified.



Assuming 80% output transformer efficiency, the transformer primary power is,

$$\text{Transformer Primary Power} = \frac{P_{FL}}{\eta_{xfmr}} = \frac{25}{0.8} = 31.25\,\text{W}.$$

For a 10% overload capacity, the power amplifier must be capable of handling

$$(110\%)(31.25) = 34.4\,\text{W}.$$

Therefore, each transistor in the Class AB push-pull amplifier must supply $34.4\,\text{W}/2 = 17.2\,\text{W}$.

The maximum collector voltage for each transistor is,

$$V_{C,\max} = V_{CC} - V_{CE(sat)} \approx V_{CC} = 24\,\text{V}.$$

For each transistor under overload conditions,

$$P_{ACper\ transistor} = \frac{V_{C,\max} I_{C,\max}}{4}.$$

Solving for $I_{C,\max}$,

$$I_{C,\max} = \frac{4P_{ACper\ transistor}}{V_{C,\max}} = \frac{4(17.2)}{24} \approx 2.87\,\text{A}.$$

Therefore, the AC load that each transistor must drive is,

$$R'_L = \frac{V_{C,\max}}{I_{C,\max}} = \frac{24}{2.87} = 8.4\ \Omega,$$

and the total primary AC load resistance is

$$R'_L = 2^2(8.4) = 33.6\,\Omega.$$

The output transformer turns ratio is then

$$\frac{n_1}{n_2} = \sqrt{\frac{R'_L}{R_L}} = \sqrt{\frac{8.36}{8}} \approx 1.$$

The full load power for each transistor is,

$$P_{FL,per\ transistor} = \frac{P_{FL}}{2} = \frac{31.25}{2} = 5.6\,\text{W}.$$

Assuming identical transistors and a base-emitter turn on voltage of $V_{BE(on)} = 0.6\,\text{V}$,

$$V_{BE(on)} = 0.6 \approx \frac{V_{CC}R_2}{R_1 + R_2} = \frac{24(600)}{R_1},$$

where $R_1 // R_2 = 600\,\Omega$.

Then $R_1 = 24\,\text{k}\Omega$ and $R_2 = 620\,\Omega$.

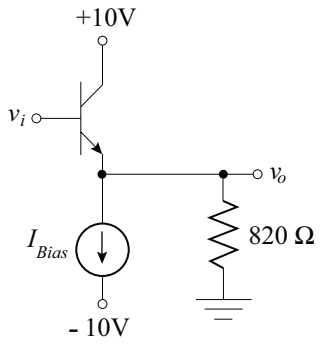
7.8 PROBLEMS

7.1. The design goals of the class A amplifier shown include:

- Maximum sinusoidal power delivered to the load of at least 40 mW, and
- Minimum possible power supply current.

Complete the design (including a realization of the current source) using a selection of resistors and BJTs with characteristics:

$$\beta_F = 150 \quad \text{and} \quad V_A = 200.$$

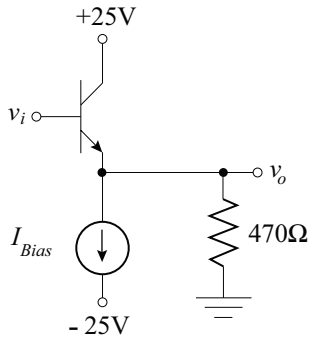


7.2. The design goals of the class A amplifier shown include:

- Maximum sinusoidal power delivered to the load of at least 0.6 W, and
- Minimum possible power supply current.

Complete the design (including a realization of the current source) using a selection of resistors and BJTs with characteristics:

$$\beta_F = 100 \quad \text{and} \quad V_A = 200.$$



7.3. A power amplifier to drive a load, $R_L = 220\,\Omega$, with the basic topology shown is under design. The Silicon power BJT is described by:

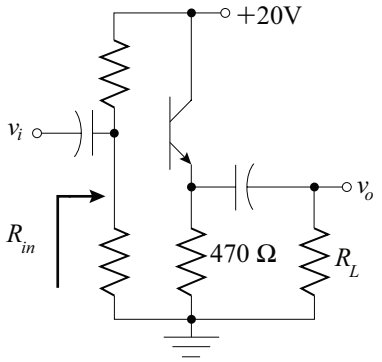
$$\beta_F = 180 \quad \text{and} \quad V_A = 100\,\text{V}.$$

The pertinent design goals are:

- maximum symmetrical output voltage swing
- $R_{in} \approx 5\,\text{k}\Omega$

(a) Complete the design by determining the proper bias resistors.

(b) Compute the maximum conversion efficiency of the design.



7.4. The amplifier of Problem 7-3 is to be redesigned for a new load, $R_L = 82\,\Omega$. The other design goals remain the same.

(a) Complete the design by determining the proper bias resistors.

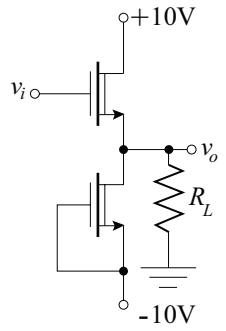
(b) Compute the maximum conversion efficiency of the design.

7.5. The common-drain class A amplifier shown uses devices for which

$$V_{PO} = -2\,\text{V} \quad I_{DSS} = 5\,\text{mA} \quad V_A = 120\,\text{V}.$$

For linear operation (the FETs must be within the saturation region), what is the range of output voltages obtained with $R_L = \infty$? What is the range for $R_L = 100\,\Omega$?

Verify the analytic results using SPICE.

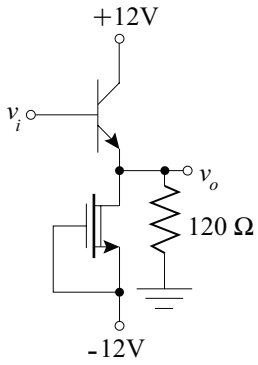


7.6. The BiFET common-emitter class A amplifier shown uses devices described by:

$$\begin{aligned} &\text{BJT:} \quad \beta_F = 150 \\ &\text{FET:} \quad V_{PO} = -2\,\text{V} \quad I_{DSS} = 7.5\,\text{mA}. \end{aligned}$$

(a) For linear operation, what is the maximum *symmetrical* range of output voltages possible?

(b) Determine the conversion efficiency when the circuit is operating with maximum symmetrical output.



7.7. Redesign the class A amplifier of Problem 7-5 by replacing the FET current with a BJT current source. For the redesigned amplifier, determine

(a) the maximum *symmetrical* range of output voltages possible maintaining linear operation?

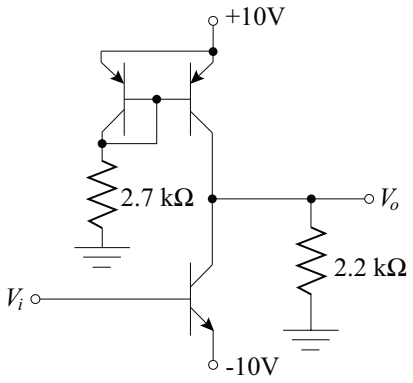
(b) the conversion efficiency when the circuit is operating with maximum symmetrical output.

7.8. The circuit shown uses BJTs described by:

$$\beta_F = 120 \quad \text{and} \quad V_A = 160\,\text{V}.$$

(a) For linear operation, what is the maximum *symmetrical* range of output voltages possible?

(b) Determine the conversion efficiency when the circuit is operating with maximum symmetrical output.

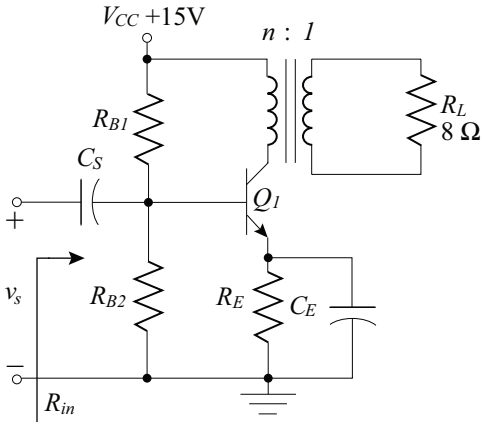


7.9. Complete the design of the Class A transformer-coupled power amplifier, shown below, to drive an 8 Ω speaker. The required input resistance of the amplifier is $R_{in} = 600\,\Omega$. The power amplifier is required to deliver 10 W of power (AC) to the 8 Ω speaker load. Design the biasing network so that a 1% change in I_C corresponds to a 10% change in β_F.

(a) Show all circuit values and the transformer turns ratio.

(b) Specify minimum transistor power dissipation rating.

(c) Confirm the operation of the design using SPICE. The transformer coupling efficiency is 0.999 and the BJT characteristics are $\beta_F = 70$, $I_S = 0.3\,\text{pA}$ and $V_A = 75\,\text{V}$.



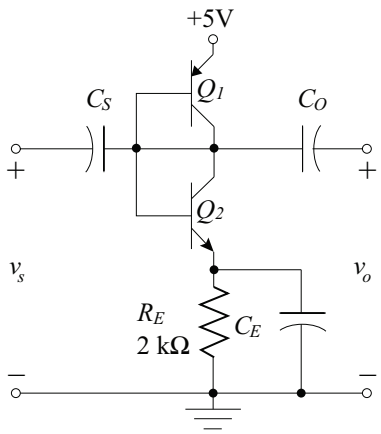
7.10. Given a Class A BJT power amplifier with a load resistance of 4 Ω and power transistor rating of

$$P_{C,\max} = 10\,\text{W},\ V_{CE(sat)} = 0.2\,\text{V}, \quad \text{and} \quad V_{CE(\max)} = 60\,\text{V},$$

(a) Determine the maximum attainable voltage swing at the output, the maximum power dissipated by the load, and the efficiency when transformer coupling is not used.

(b) Repeat part (a) when a transformer coupling is used with a transformer turns ratio of 2.

7.11. For the complementary push-pull amplifier shown below, determine the peak-to-peak voltage of the largest possible undistorted sinusoidal output. The Silicon transistor is described by $\beta_F = 75$.



7.12. For the Class B amplifier shown, find the following:

(a) maximum undistorted peak output voltage

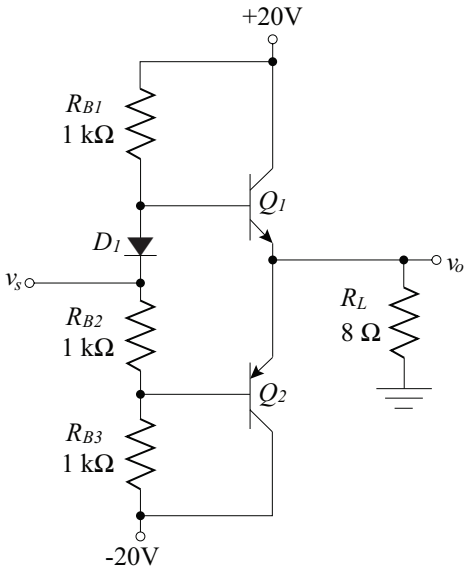
(b) maximum DC power consumed

(c) output AC power

(d) the maximum amplifier efficiency, η.

Assume that the transistors are matched with

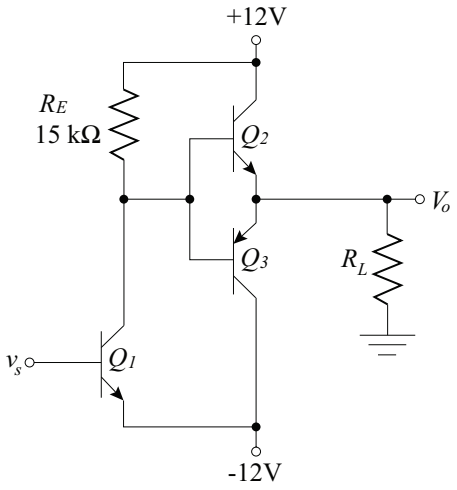
$$\beta_F = 100,\ I_S = 0.03\,\text{pA} \quad \text{and} \quad V_{\gamma D1} = 0.7\,\text{V}.$$



7.13. The push-pull power amplifier shown uses identical transistors with $\beta_F = 75$. Find the maximum positive and negative values of V_o for:

(a) $R_L = 10\,\text{k}\Omega$

(b) $R_L = 1\,\text{k}\Omega$.



7.14. The common-drain class B amplifier shown uses devices for which

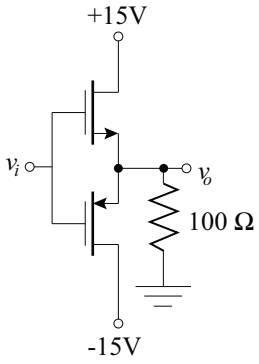
$$V_T = 1\,\text{V} \quad \text{and} \quad K = 200\,\mu\text{A/V}^2.$$

For a sinusoidal input,

(a) at what input voltages do the respective FETs enter the saturation region?

(b) what is the maximum peak output voltage level?

(c) what is the maximum conversion efficiency of this circuit?



7.15. Complete the design of the Class B push-pull amplifier, shown below, which uses matched BJTs with $\beta_F = 75$, $I_S = 0.03\,\text{pA}$ and $V_A = 120\,\text{V}$. Assume 99% transformer efficiency, rated load power of 12 W, and an overload capacity of 10%.

(a) Determine the input transformer ratio, n_p, for maximum power transfer.

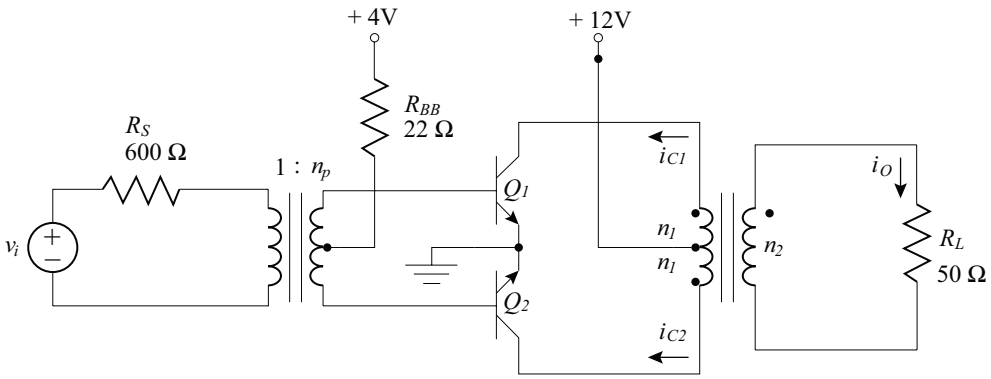
(b) Determine the output transformer ratio, $n_1 : n_2$.

(c) Find the maximum values of i_{C1}, i_{C2}, and i_o.

(d) Find the power delivered to the load per transistor, $P_{ACper\,transistor}$, collector power dissipation, P_C, and DC power dissipation, P_{DC}.

(e) Calculate the amplifier efficiency, η.

(f) Plot the transfer characteristic of the power amplifier using SPICE.

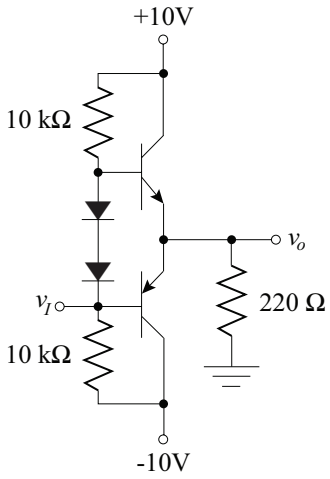


7.16. The class AB amplifier shown uses two 10 kΩ resistors to establish quiescent current through two diodes bridging the base-emitter junctions of a matched BJT pair. This quiescent current increases the DC power drawn from the power supplies and therefore decreases the efficiency of the amplifier. The transistors have characteristics:

$$\beta_F = 150 \quad \text{and} \quad V_A = 200.$$

(a) Determine the maximum conversion efficiency.

(b) What is the conversion efficiency if the output is reduced to one-half the maximum possible undistorted amplitude?



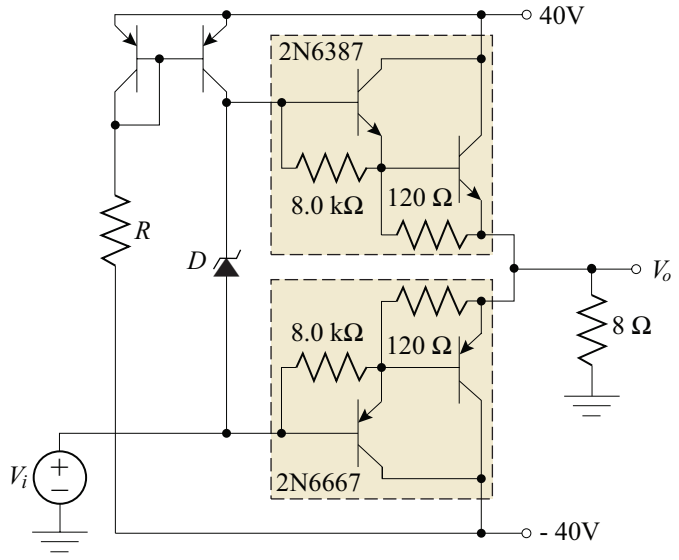
7.17. A class AB amplifier with the general topology shown at the right is under design. The power transistors being used are Silicon Darlington pairs (shown in schematic form). A Zener diode is being used to eliminate crossover distortion and a current source provides biasing.

(a) What should the Zener voltage, V_z, be to eliminate crossover distortion?

(b) What is the maximum sinusoidal amplitude of the output voltage?

(c) The typical DC current gain of the Darlington pairs is 2500, and the Zener diode requires a minimum diode current of 2 mA to ensure regulation. What is the maximum value of the resistor, R, necessary to keep the Zener diode in regulation while achieving maximum output power?

(d) Determine the maximum efficiency of this circuit with the above determined diode, transistor, and resistor parameters.



7.18. A class AB amplifier with the general topology shown is under design. The transistors being used are Silicon Darlington pairs (shown in schematic form). A Zener diode is being used to eliminate crossover distortion. This Zener diode requires a minimum diode current of 500 μA to ensure regulation. The individual BJTs in the Darlington pairs are Silicon with $\beta_F = 60$.

(a) What should the diode Zener voltage, V_z, be in order to eliminate crossover distortion?

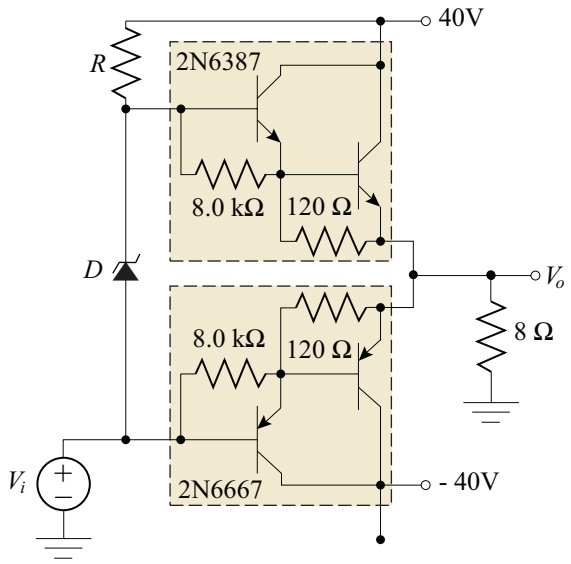
(b) If the design goals include delivering 55 W of signal power to the load, what is the minimum undistorted output voltage swing?

(c) For purposes of simple analysis, the resistors shunting the BJT base-emitter junctions can be considered to act as current sources of value:

$$I_{Bias} = \frac{V_\gamma}{R_{shunt}}.$$

Determine the maximum value of the resistor labeled "R" to meet the design goal (55 W of signal power delivered to the load).

(d) Determine the maximum efficiency of this circuit using the design value of the resistor determined in part c and the Zener voltage determined in part (a).



7.19. Complete the design of the Class AB power amplifier, shown below, which uses matched BJTs with $\beta_F = 50$, $I_S = 0.3\,\text{pA}$ and $V_A = 150\,\text{V}$. Assume 99% transformer efficiency, rated load power of 15 W, and an overload capacity of 15%.

(a) Determine the input transformer ratio, n_p, for maximum power transfer.

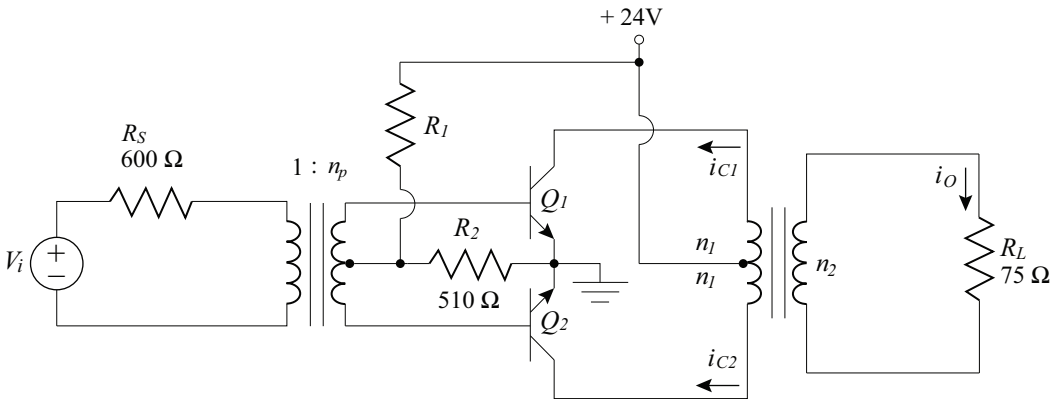
(b) Determine the output transformer ratio, $n_1 : n_2$.

(c) Find the maximum values of i_{C1}, i_{C2}, and i_o.

(d) Find the power delivered to the load per transistor, $P_{AC\,per\,transistor}$, collector power dissipation, P_C, and DC power dissipation, P_{DC}.

(e) Calculate the amplifier efficiency, η.

(f) Plot the transfer characteristic of the power amplifier using SPICE.

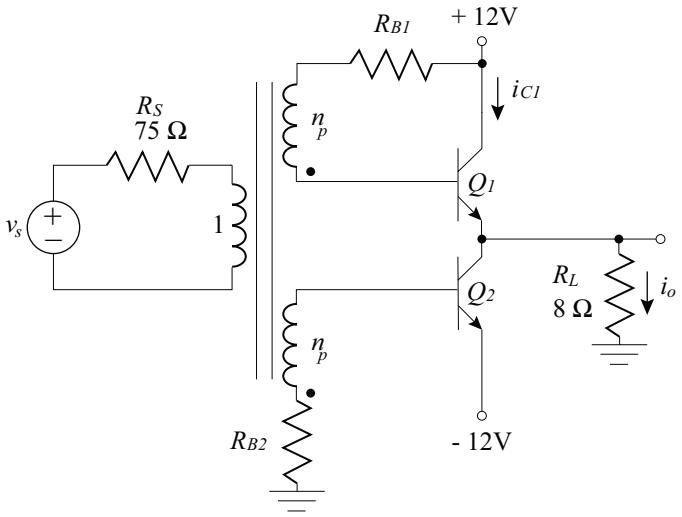


7.20. Complete the design of a direct-coupled output push-pull amplifier, shown to achieve a maximum output to an 8 Ω load. The circuit uses matched transistors with the following specifications:

$$P_{C,\max} = 8\,\text{W}, \quad i_{C,\max} = 1.5\,\text{A}, \quad \beta_F = 60,$$
$$V_A = 120\,\text{V}, \quad I_S = 0.05\,\text{pA} \quad \text{and} \quad V_{CE,\max} = 55\,\text{V}.$$

(a) Determine the maximum input voltage for an undistorted output signal.

(b) Plot the transfer characteristic of the power amplifier using SPICE.



7.21. Design a Class B power amplifier stage to deliver an average power of 75 W into a 12 Ω load. The power supply must be 5 volts greater than the peak sinusoidal output signal.

(a) Draw the schematic of the power amplifier.

(b) Determine the required power supply voltage, peak power supply current, total DC power consumed by the circuit, and efficiency of the amplifier.

(c) Determine the maximum possible power dissipation per transistor for a sinusoidal input signal.

7.22. Design a Class AB direct-coupled output power amplifier using matched BJTs with $\beta_F = 60, I_S = 0.05\,\text{pA}$ and $V_A = 120\,\text{V}$. The amplifier is required to provide a rated load power of 15 W, and an overload capacity of 15%. Assume 99% transformer efficiency and a power supply of $\pm 24\,\text{V}$.

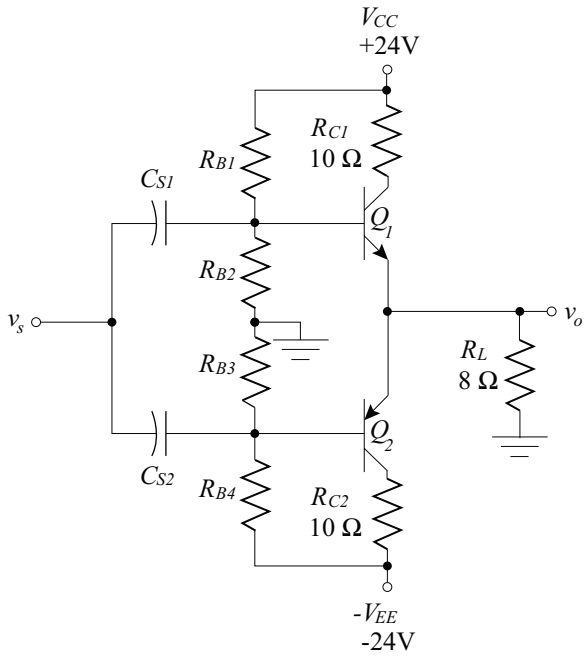
7.23. Complete the design of the Class AB power amplifier shown below for $R_{B1}//R_{B2} = R_{B3}//R_{B4} = 12\,\text{k}\Omega$. The transistors are matched and have the parameters $\beta_F = 60, I_S = 0.033\,\text{pA}$ and $V_A = 120\,\text{V}$.

(a) Design the bias network to eliminate crossover distortion (adjust to $V_{BE(on)} = 0.6\,\text{V}$).

(b) What is the maximum undistorted power delivered to the load?

(c) Determine the DC power dissipation, P_{DC}, and the efficiency, η, of the amplifier for maximum output current.

(d) Plot the transfer characteristic of the power amplifier using SPICE.



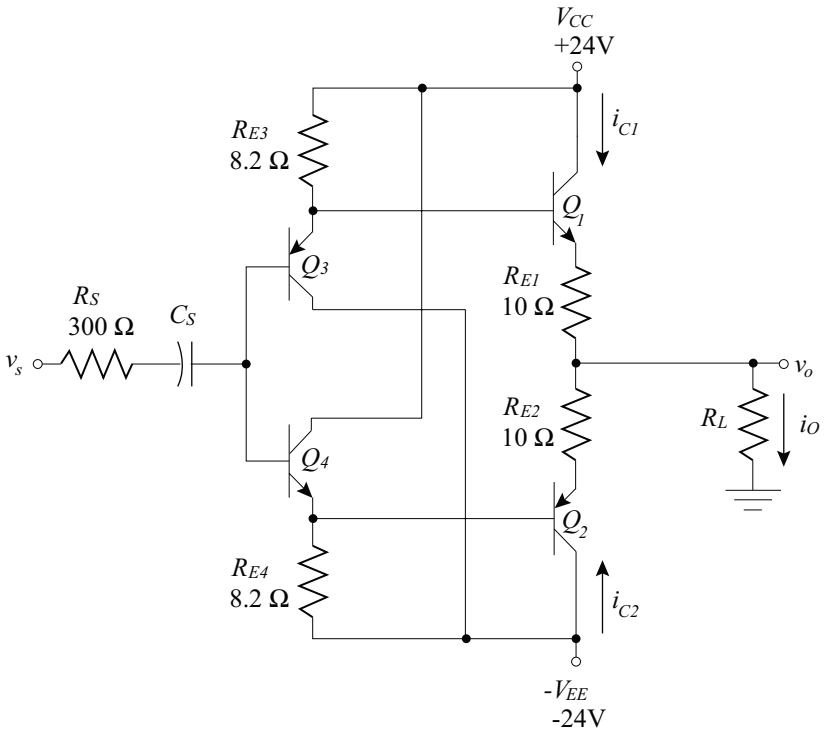
7.24. A direct-coupled Class-AB power amplifier is shown below using matching transistors with parameters $\beta_F = 75$, $I_S = 0.033\,\text{pA}$, and $V_A = 100\,\text{V}$. Resistors R_{E1} and R_{E2} are included to guard against the possibility of transistor thermal runaway.

(a) For $R_L = \infty$, find the quiescent current through each transistor and calculate v_o.

(b) For $R_L = \infty$, find the collector current through each transistor when $v_s = +5\,\text{V}$ and calculate v_o.

(c) For $R_L = 75\,\Omega$, find the collector current through each transistor when $v_s = +5\,\text{V}$ and calculate v_o.

(d) Plot the transfer characteristic of the amplifier using SPICE for $R_L = 75\,\Omega$.

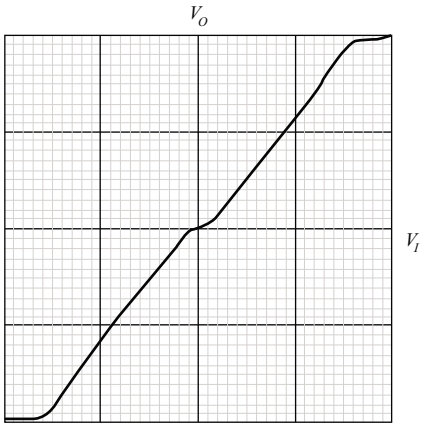


7.25. A class B amplifier has the transfer characteristic shown. Determine the second and third harmonic distortion (in dB) and the total harmonic distortion for the following amplitude input sinusoids:

(a) $14\cos(\omega t)$ V

(b) $8\cos(\omega t)$ V

The scale is 10 V/major division.

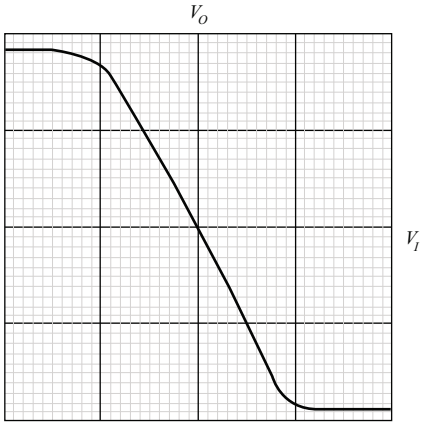


7.26. A class A amplifier has the transfer characteristic shown (the quiescent point for the amplifier is the central point the diagram). Determine the second and third harmonic distortion (in dB) and the total harmonic distortion for the following amplitude input sinusoids:

(a) $0.1\cos(\omega t)$ V

(b) $0.2\cos(\omega t)$ V

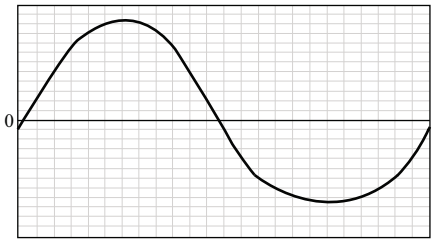
The vertical scale is 5 V/major division and the horizontal scale is 0.2 V/major division.



7.27. The input to an amplifier is a pure, undistorted sinusoid. One cycle of the resultant output waveform is shown. The vertical scale is 1 V/div. and the horizontal scale is 50 μs/div.

(a) Determine the amplifier second and third harmonic distortion by sampling the waveform at appropriately positioned data points and performing appropriate calculations.

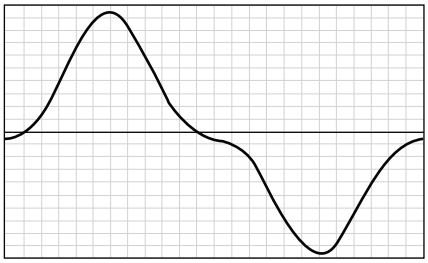
(b) What is the total harmonic distortion of the amplifier with this input?



7.28. The input to an amplifier is a pure, undistorted sinusoid. One cycle of the resultant output waveform is shown. The vertical scale is 0.5 V/div. and the horizontal scale is 20 ms/div.

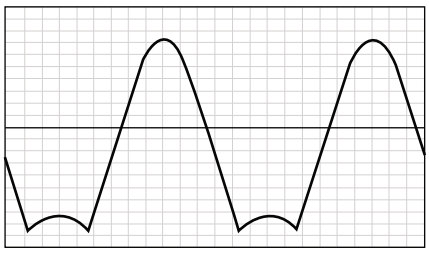
(a) Determine the amplifier second and third harmonic distortion by sampling the waveform at appropriately positioned data points and performing appropriate calculations.

(b) What is the total harmonic distortion of the amplifier with this input?



7.29. Amplifiers may distort the input signal in rather unusual ways. For instance a Class A, common-emitter amplifier with an emitter resistor responds to an overly-large input as show.

Determine the second, third, and total harmonic distortion of the output waveform shown.



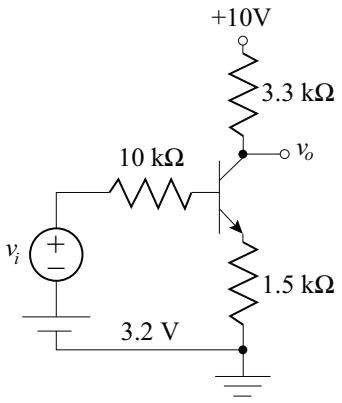
7.30. A Class A, common-emitter amplifier with an emitter resistor responds to an overly-large amplitude input signal by "reflecting" a portion of the signal (see output waveform shown in the previous problem). This "reflection" occurs while the BJT is in the saturation region of operation. Investigate this phenomenon by using simple BJT regional models to analyze the output voltage waveform of circuit shown for the following amplitude input sinusoids:

(a) $v_i(t) = 0.5\sin(\omega t)$

(b) $v_i(t) = 1.5\sin(\omega t)$

(c) $v_i(t) = 3.0\sin(\omega t)$

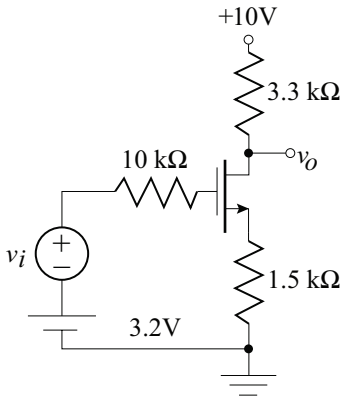
The Silicon BJT is described by $\beta_F = 100$.



7.31. Perform the distortion investigation of the circuit shown in the previous problem using SPICE. Comment on results.

7.32. It seems reasonable to assume that the "reflection" distortion found in common-emitter amplifiers with an emitter resistor might also be present in common-source amplifiers with a source resistor. Investigate the distortion present in the FET circuit shown using SPICE and compare results to those found in Problems 7-27 or 7-28. Comment on the similarities and/or differences in the output of the two circuits. Explain what characteristics in FET and BJT performance cause these similarities and/or differences. The FET in the given circuit is described by:

$$V_T = 1.0\,\text{V} \quad K = 5\,\text{mA}/V^2 \quad V_A = 160\,\text{V}.$$



7.33. An amplifier is characterized using the two tone measurement method with a total average input power of 100 μW. The resulting intermodulation results were: $IMD_2 = -35$ dB and $IMD_3 = -40$ dB. The amplifier is not experiencing gain compression.

(a) Find the second and third harmonic ratios (to the fundamentals).

(b) Determine the Fourier coefficients of the output signal.

(c) Use SPICE or other computer software package to plot the transfer function of the output compared to the ideal undistorted transfer characteristic.

(d) Maintaining a 5 dB difference in IMD_2 and IMD_3, determine the distortion level where there is a 5% difference between the transfer function of the amplifier and the ideal.

7.34. Consider the Class-B push-pull amplifier shown in Figure 7.33. The amplifier distortion characteristics are given as $IMD_2 = -30$ dB and $IMD_3 = -40$ dB for the input signal power used.

(a) If the base current in Q_1 is $i_{B1} = I_{B1}(\cos\omega_o t + 0.02\cos 2\omega_o t)$, find the corresponding Q_2 collector current and the total output current at the load.

(b) If the base current in Q_1 is $i_{B1} = I_{B1}(\cos\omega_o t + 0.02\cos 3\omega_o t)$, find the corresponding Q_2 collector current and the total output current at the load.

(c) Use SPICE to simulate parts (a) and (b). The transistors are matched with parameters $\beta_F = 75$, $I_S = 0.033$ pA, and $V_A = 100$ V.

7.35. Data from a transistor specification sheet shows that the maximum junction temperature is 150°C and the maximum allowable dissipation at any temperature is 15 W. The transistor should be derated above 25°C ambient. Assume a heat sink is used with $\theta_{cs} = 0.7$°C/W and $\theta_{sa} = 1.5$°C/W. Let $P_D = 7$ W at a 40°C ambient. Find:

(a) the junction temperature

(b) the case temperature

(c) the heat sink temperature.

7.36. A thermal equivalent circuit has $\theta_{sa} = 0.2°C/mW$, $\theta_{cs} = 0.1°C/mW$, and $\theta_{jc} = 0.1°C/mW$ for a particular transistor.

(a) If the thermal system (transistor and heat sink) dissipates 0.1 W into an ambient environment at 30°C, find the junction temperature, T_j, case temperature, T_c, and heat sink temperature, T_s.

(b) If $T_j = 150°C$ with $T_A = 50°C$, find T_C and P_D.

7.37. A typical transistor may have thermal data as follows: "Total device dissipation at $T_A = 25°C$ is 1 W; derate above 25°C, 10 mW/°C." What is the safe power dissipation at an ambient temperature of

(a) 75°C

(b) 0°C

(c) If $\theta_{jc} = 0.03°C/mW$, what is θ_{ca} (case-to-ambient thermal resistance)?

7.38. Given a BJT with the following parameters:

$$\beta_F = 75,\ I_S = 0.033\,pA, \quad \text{and} \quad V_A = 100\,V,$$

and a power supply voltage of 15 V: Assume that the BJT SPICE parameters XTB = 1.5 and XTI = 3 yielding $V_{BE} = 0.7\,V$ @ 25°C and decreasing linearly by 1.3 mV/°C.

(a) Design a stable biasing circuit for $I_C = 5\,mA \pm 0.05\,mA$ and $V_{CE} = 5\,V \pm 1\,V$ for $-55°C \leq T \leq 125°C$. Assume that the BJT SPICE parameters XTB = 1.5 and XTI = 3 yielding, $V_{BE} = 0.7\,V$@25°C and decreasing linearly by 1.3 mV/°C.

(b) Find the junction temperature at ambient temperatures of −55°C and 125°C.

7.39. A transistor is specified for a maximum allowable case temperature of 150°C. The maximum allowable dissipation is 150 mW, and the transistor should be derated above $T_C = 25°C$. If $\theta_{cs} = 0.1°C/mW$ and $\theta_{sa} = 0.4°C/mW$, find the temperature of the heat sink when:

(a) 150 mW is being dissipated and $T_C = 25°C$

(b) 150 mW is being dissipated and $T_C = 0°C$

(c) as much power as possible is being dissipated and $T_C = 100°C$.

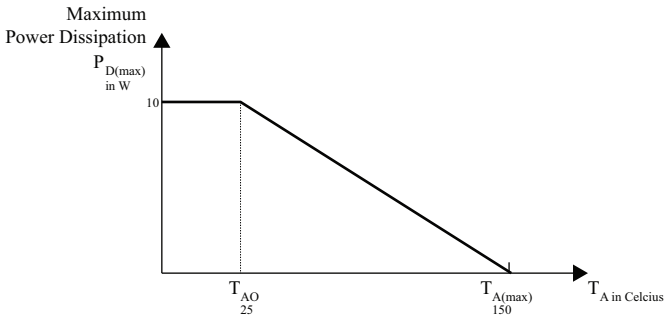
7.40. The given power derating curve of a FET shows maximum power dissipation as a function of ambient temperature. If $\theta_{ca} = 2°C/mW$, find:

(a) θ_{ja}

(b) θ_{jc}

(c) What is the maximum safe value of P_D if $T_A = 100°C$?

(d) How much power may be dissipated if $T_C = 100°C$?



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CHAPTER 8

Feedback Amplifier Principles

Feedback is the process of combining a portion of the output of a system with the system input to achieve modified performance characteristics. Negative feedback is especially import in amplifier design as it produces several significant benefits. The primary *benefits* are:

- The gain of the amplifier is stabilized against variation in the characteristic parameters of the active devices due to voltage or current supply changes, temperature changes, or device degradation with age. Similarly, amplifier performance is stabilized within a group of amplifiers that have, by necessity, active devices with different characteristic parameters.
- The input and output impedances of the amplifier can be selectively increased or decreased.
- Non-linear signal distortion is reduced.
- The midband frequency range is increased. Discussion of this aspect is delayed until Chapter 11 (Book 3).

It is a rare occurrence when benefits come without a price. In the case of negative feedback, the above listed benefits are accompanied by two primary *drawbacks:*

- The gain of the circuit is reduced. In order to regain the losses due to feedback, additional amplification stages must be included in the system design. This adds complexity, size, weight, and cost to the final design.
- There is a possibility for oscillation to occur. Oscillation will destroy the basic gain properties of the amplifier. Discussion of this aspect will also be delayed until Chapter 11 (Book 3).

In this chapter the benefits of negative feedback are considered. Basic definitions are followed by a general discussion of the properties of a feedback system. Amplifiers are divided into four categories of feedback topology and the specific properties of each topological type are derived. While the emphasis of discussions must focus on circuit analysis techniques, a clear understanding of the of feedback in general, and effects of circuit topology in particular, is a necessity for good feedback amplifier design.

The Summary Design Example explores the common design practice of modifying existing circuitry to meet new, but similar, performance specifications. Minimal alteration of the existing design is explored as a possible, discretionary design criterion.

8.1 BASIC FEEDBACK CONCEPTS

The basic topology of a feedback amplifier is shown in Figure 8.1. This figure shows a feedback system in its most general form: each signal symbolized with $\{X_{()}\}$ can take the form of either a voltage or a current, and travels only in the direction of the indicated arrows. The triangular symbol is a linear amplifier of gain, A, as has been described in several of the preceding Chapters. The rectangle indicates a feedback network that samples the output signal, scales it by a factor, f, and passes it forward to the input of the system. The circular symbol is a summing (or *mixing*) junction that subtracts the feedback signal, X_f, from the inputs. Subtraction of the two inputs at the summing junction is a key factor in negative feedback systems.

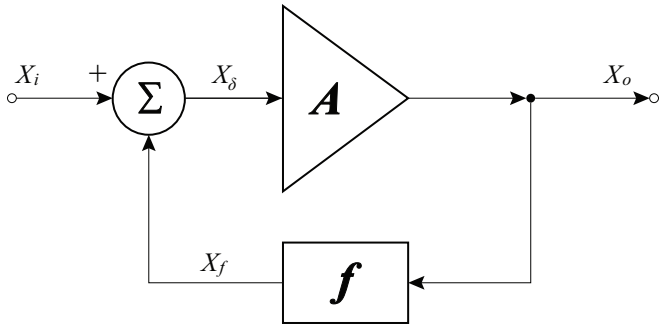


Figure 8.1: Basic negative feedback topology.

The system can be mathematically modeled in the following fashion. The output of the amplifier, X_o, is related to its input signal X_δ by a linear amplification factor (gain), A, often called the *forward or open-loop gain:*

$$X_o = A(X_\delta). \tag{8.1}$$

Since the quantities X_o and X_δ can be either voltage or current signals, the forward gain, A, can be a voltage gain, a current gain, a transconductance, or a transresistance.[1] The feedback signal, X_f (a fraction of the output signal, X_o) is then subtracted

$$X_\delta = (X_i - X_f) = (X_i - fX_o), \tag{8.2}$$

where f is the feedback ratio defining the relationship between X_f and X_o:

$$X_f = fX_o. \tag{8.3}$$

The feedback ratio, f, can also be a ratio of voltages, currents, transconductance, or transresistance. *In order to have stable negative feedback, it is necessary that the mathematical sign of f be the same as that of A.*[2] Thus, the product, Af, called the *loop gain*, is a positive, dimensionless quantity.

[1] Gain quantities are ratios of an output quantity to an input quantity. Transresistance implies the ratio of an output voltage to an input current: transconductance is the ratio of an output current to an input voltage.

[2] This mathematical sign identity is necessary in the midband frequency region: Chapter 11 (Book 3) explores frequency-dependent phase shifts in the gain and feedback quantities and their consequences.

The input-output relationship for the overall system is derived from Equations (8.1) and (8.2):

$$X_o = \frac{A}{1 + A\,f} X_i = A_f X_i. \tag{8.4}$$

The overall gain of the system including the effects of feedback is then written as:

$$A_f = \frac{X_o}{X_i} = \frac{A}{1 + A\,f}. \tag{8.5}$$

Notice that A_f does not need to be either a voltage or current gain: it will have the same dimensions as the forward gain, A. Equation (8.5) has special significance in the study of feedback systems and is called the *basic feedback* equation. The denominator of the basic feedback equation is identified as the *return difference*, D, also referred to as the amount of feedback:

$$D = 1 + Af. \tag{8.6}$$

The return difference, for negative feedback systems, has magnitude larger than unity (in the midband frequency region) and is often specified in decibels:

$$D_{\text{dB}} = 20 \log_{10} |1 + Af|. \tag{8.7}$$

The return difference quantifies the degradation in gain due to the addition of feedback to the system. It also plays a significant role in quantifying changes in input and output impedance and frequency bandwidth.

The derivation of the basic feedback equation is based on two basic idealized assumptions:

- The reverse transmission through the amplifier is zero (applying a signal at the output produces no signal at the input).
- The forward transmission (left to right in Figure 8.1) through the feedback network is zero.

While these assumptions are impossible to meet in practice, a reasonable approximation is obtained with the following realistic requirements:

- The reverse transmission through the amplifier is negligible compared to the reverse transmission through the feedback network.
- The forward transmission through the feedback network is negligible compared to the forward transmission through the amplifier.

In most feedback amplifiers the amplifier is an active device with significant forward gain and near-zero reverse gain; the feedback network is almost always a passive network. Thus, in the forward direction, the large active gain will exceed the passive attenuation significantly. Similarly, in the reverse direction, the gain of the feedback network, albeit typically small, is significantly

greater than the near-zero reverse gain of the amplifier. In almost every electronic application, the above stated requirements for the use of the basic feedback equation are easily met by the typical feedback amplifier.

Some of the drawbacks and benefits of feedback systems can be investigated on a simple level by looking at the properties of the basic feedback equation (Equation (8.5)):[3]

1. *The gain of the circuit is reduced.* It has been already shown that the overall gain is the gain of the simple amplifier without feedback divided the return difference, which is larger in magnitude than one.

2. *There is a possibility for oscillation to occur.* It will be shown in Chapters 10 and 11 (Book 3) that the gain decreases and the phase of the gain of an amplifier changes as frequency increases. This change in phase may cause the loop gain, Af, to change sign from positive to negative. If this change in sign occurs at the same frequency that the magnitude of the loop gain approaches unity, the return difference approaches zero at that frequency. Division by zero indicates an instability: that instability is realized as an oscillation. Linear oscillators are discussed in Chapter 12 (Book 4).

3. *The gain of the amplifier is stabilized against variation in the characteristic parameters of the active devices.* It has been shown in previous chapters, that the gain, A, of an amplifier is highly dependent on the parameters of the active devices. These parameters are highly dependent on temperature, bias conditions, and manufacturing tolerances. It is therefore desirable to design amplifiers that are reasonably insensitive to the variation of the device parameters.

The relationship between the differential change in gain due to device parameter variation with and without feedback is obtained by differentiating Equation (8.5):

$$d\,A_f = \frac{1}{(1 + A\,f)^2} d\,A, \tag{8.8}$$

which is more typically expressed as:

$$\left|\frac{d\,A_f}{A_f}\right| = \left|\frac{1}{(1 + A\,f)}\right| \left|\frac{d\,A}{A}\right|. \tag{8.9}$$

Stable negative feedback amplifiers require that the return difference have magnitude greater than unity:

$$(1 + Af) > 1; \tag{8.10}$$

[3]The change in the input and output impedances can not be investigated at this level: it is necessary to specify the nature (voltage or current) of the input and output quantities. Discussion of these properties of feedback systems is found in Section 8.3.

thus the variation of the overall amplifier gain, A_f, is reduced by a factor of the return ratio.

Example 8.1
A feedback amplifier is constructed with an amplifier that is subject to a 3% variation in gain as its fundamental forward-gain element. It is desired that the feedback amplifier have no more than 0.1% variation in its overall gain due to the variation in this element. Determine the necessary return difference to achieve this design goal.

Solution:

Equation (8.9) is the significant relationship:

$$\left|\frac{d\,A_f}{A_f}\right| = \left|\frac{1}{(1+A\,f)}\right|\left|\frac{d\,A}{A}\right|.$$

The significant properties are:

$$0.001 \;\geq\; \left|\frac{1}{(1+A\,f)}\right| 0.03 \qquad \Rightarrow \qquad D = 1 + A\,f \geq 30.$$

The minimum necessary return ratio is 30: more often identified as its decibel equivalent,

$$D_{\text{dB}} = 20\log_{10} D = 29.54\,\text{dB}.$$

Equation (8.9) is useful for small changes in amplification due to parameter variation. If the change are large, the mathematical process must involve differences rather than differentials:

$$\Delta A_f = A_{2f} - A_{1f} = \frac{A_2}{1+A_2 f} - \frac{A_1}{1+A_1 f}. \tag{8.11}$$

In order to put this into the same format as Equation (8.9), it is necessary to divide both sides of the equation by A_{1f}:

$$\left|\frac{\Delta A_f}{A_{1f}}\right| = \left|\frac{A_2}{1+A_2 f}\left(\frac{1+A_1 f}{A_1}\right) - 1\right| = \left|\frac{(A_2 - A_1)}{1+A_2 f}\left(\frac{1}{A_1}\right)\right|, \tag{8.12}$$

or

$$\left|\frac{\Delta A_f}{A_{1f}}\right| = \left|\frac{1}{1+A_2 f}\right|\left|\frac{\Delta A}{A_1}\right| = \left|\frac{1}{1+(A_1+\Delta A)\,f}\right|\left|\frac{\Delta A}{A_1}\right|. \tag{8.13}$$

Example 8.2
A feedback amplifier is constructed with an amplifier with nominal gain, $A = 100$, that is subject to a 30% variation in gain as its fundamental forward-gain element. It is desired that the feedback

amplifier have no more than 1% variation in its overall gain due to the variation in this element. Determine the necessary return difference to achieve this design goal.

Solution:

This problem statement is a duplicate of Example 8.1 with the variation increased by a factor of 10. Use of Equation (8.9) will produce the same results ($D = 30$). The large variation, however, requires the use of Equation (8.13)

$$|0.01| \geq \left| \frac{1}{1 + (A_1 + \Delta A)f} \right| |0.3| \qquad \Rightarrow \qquad 1 + (A_1 + \Delta A)f \geq 30,$$

where $A_1 = 100$ and $\Delta A = \pm 0.3(A_1) = \pm 30$. Solving the above inequality using both values of ΔA leads to two values of the feedback ratio, f:

$$f \geq 0.2231 \quad \text{or} \quad f \geq 0.4143.$$

Good design practice indicates that *both* inequalities should be satisfied. Thus,

$$D = (1 + A_1 f) = (1 + 100\{0.4143\}) = 42.43,$$

and

$$D_{\text{dB}} = 20 \log_{10} D = 32.55 \,\text{dB}.$$

This result is about 3 dB more than predicted using the methods in Example 8.1.

---

4. *Non-linear signal distortion is reduced.* Stabilization of gain with parameter variation suggests that the gain will be stabilized with respect to other gain-changing effects. One such effect is non-linear distortion: this type of distortion is a variation of the gain with respect to input signal amplitude. A simple example of non-linear distortion is shown in Figure 8.2. Here the transfer characteristic of a simple amplifier is approximated by two regions, each of which is characterized by different amplification, A_1 and A_2. To this transfer characteristic, a small amount of feedback is applied so that $A_1 f = 1$, and the resultant feedback transfer characteristic is also shown.

   As can be easily seen, the overall feedback transfer characteristic also consists of two regions with overall amplification A_{1f} and A_{2f}. In this demonstration, the amplification ratios are:

$$\frac{A_1}{A_2} = 3 \qquad \text{and} \qquad \frac{A_{1f}}{A_{2f}} = 1.5.$$

   Feedback has significantly improved the linearity of the system and reduced non-linear distortion. Larger amounts of feedback (increasing the feedback ratio, f) will continue to

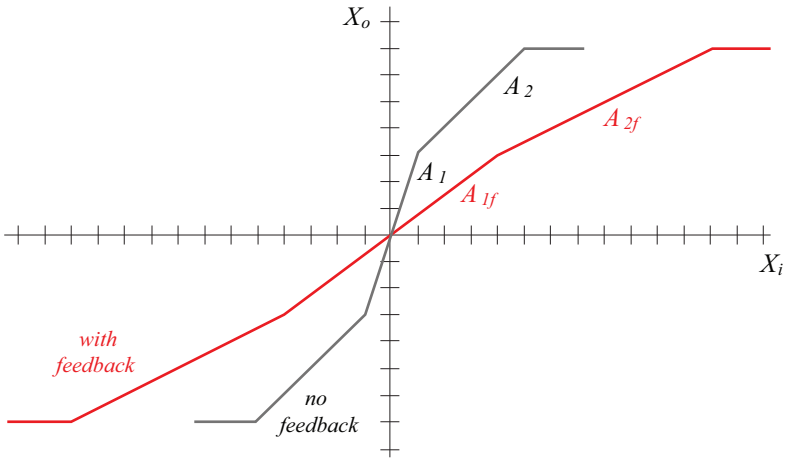


Figure 8.2: The effect on feedback on an amplifier transfer characteristic.

improve the linearity. For this example, increasing the feedback ratio by a factor of 5 will result in a ratio of overall gain in the two regions of 1.067 (as compared to 1.5, above).

It should be noted that the saturation level of an amplifier is not significantly altered by the introduction of negative feedback. Since the incremental gain in saturation is essentially zero, the feedback difference is also zero. No significant change to the input occurs and the output remains saturated.

Another possible viewpoint on gain stabilization comes from another form of the basic feedback equation:

$$A_f = \frac{A}{1 + A\,f} = \frac{1}{f}\left(1 - \frac{1}{1 + A\,f}\right) \approx \frac{1}{f}. \tag{8.14}$$

For large return difference ($D = 1 + Af$) the overall gain with feedback is dominated by the feedback ratio, f.

5. *The midband frequency range is increased.* While this property is discussed extensively in Chapter 11 (Book 3), it can be considered a special case of the reduction in gain variation. As frequencies increase, the performance parameters of an amplifier degrade. Similarly, coupling and bypass capacitors will degrade low-frequency performance. Feedback reduces the effects of these frequency-dependent degradations and thereby increases the frequency band over which the amplifier has stable gain.

8.2 FEEDBACK AMPLIFIER TOPOLOGIES

As has been seen in the previous section, general discussions provide great insight into many of the properties of feedback systems. In order to consider the design of electronic *feedback amplifiers,* it is necessary, however, to specify the details of the feedback sampling and mixing processes and the circuits necessary to accomplish these operations. The sampling and mixing processes have a profound effect on the input impedance, the output impedance, and the definition of the forward gain quantity that undergoes *quantified* change due to the application of feedback.[4] This section will analyze the various idealized feedback configurations: Section 8.3 will look at practical feedback configurations.

As has been previously stated, both the mixing and the sampling process for a feedback amplifier can utilize either voltages or currents. Voltage mixing (subtraction) implies a series connection of voltages at the input of the amplifier: current mixing implies a shunt connection. Voltage sampling implies a shunt connection of the sampling probes across the output voltage: current sampling implies a series connection so that the output current flows into the sampling network. Either type of mixing can be combined with either type of sampling. Thus, a feedback amplifier may have one of four possible combinations of the mixing and sampling processes. These four combinations are commonly identified by a hyphenated term: (mixing topology)-(sampling topology). The four types are:

- *shunt-shunt feedback* (current mixing & voltage sampling)
- *shunt-series feedback* (current mixing & current sampling)
- *series-shunt feedback* (voltage mixing & voltage sampling)
- *series-series feedback* (voltage mixing & current sampling)

The four basic feedback amplifier topologies are shown schematically in Figure 8.3. A source and a load resistance have been attached to model complete operation. In each diagram the input, feedback and output quantities are shown properly as voltages or currents. Forward gain, A, must be defined as the ratio of the output sampled quantity divided by the input quantity that undergoes mixing. As such it is a transresistance, current gain, voltage gain, or transconductance. The feedback network, as described by the feedback ratio (f), must sample the output quantity and present a quantity to the mixer that is of the same type (current or voltage) as the input quantity. As such it is a transconductance, current gain, voltage gain, or transresistance. Table 8.1 is listing of the appropriate quantities mixed at the input, the output sampled quantity, the forward gain, and the feedback ratio for each of the four feedback amplifier topologies. It is important to remember that the product, Af, must be dimensionless and, in the midband region of operation, positive.

[4]For any gain topology, all forward gain quantities may undergo change: the gain quantity listed in Table 8.1 is the single quantity that is altered as described by the basic feedback equation (Equation (8.5)).

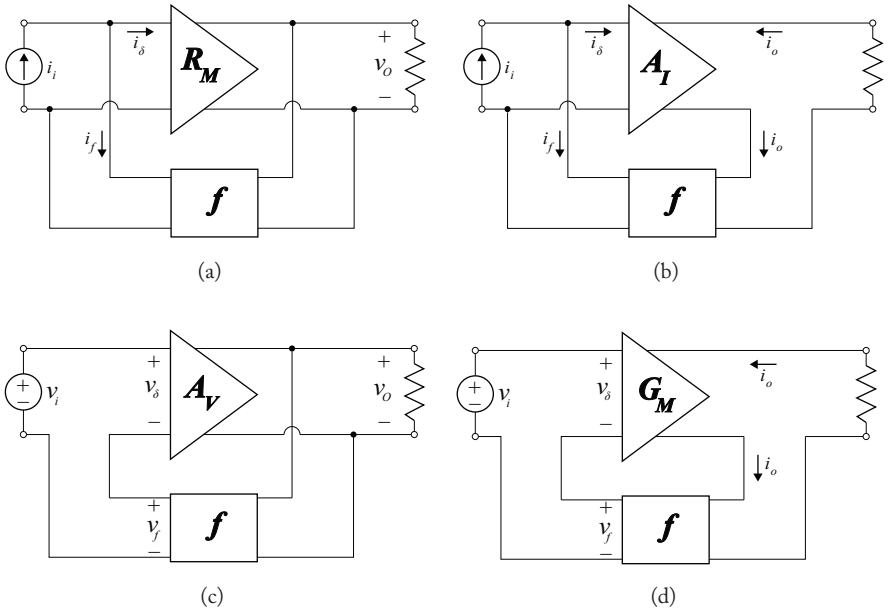


Figure 8.3: Feedback amplifier topologies (a) shunt-shunt feedback; (b) shunt-series feedback; (c) series-shunt feedback; and (d) series-series feedback.

Table 8.1: Feedback amplifier topology parameters

	shunt-shunt	*shunt-series*	*series-shunt*	*series-series*
input, X_i	current, i_s	current, i_s	voltage, v_s	voltage, v_s
output, X_o	voltage, v_o	current, i_o	voltage, v_o	current, i_o
forward gain, A	transresistance, R_M	current gain, A_I	voltage gain, A_V	transconductance, G_M
feedback ratio, f	i_f/v_o	i_f/i_o	v_f/v_o	v_f/i_o

In the previous section, all drawbacks and benefits of feedback were discussed *except* the modification of input and output impedance. The specific definitions of the four feedback amplifier topologies allow for that discussion to begin here. The *mixing process alters the input impedance*

of a negative feedback amplifier. Shunt mixing decreases the input resistance and series mixing increases the input impedance.

1. *Shunt mixing decreases the input resistance.* For the *shunt-shunt* feedback amplifier (Figure 8.4), the voltage across its input terminals (arbitrarily identified as v) and the input current, i_i, are related by the feedback amplifier input resistance, R_{if}:

$$v = i_i R_{if}. \tag{8.15}$$

Similarly, the forward gain amplifier has input quantities related by its input impedance, R_i:

$$v = i_\delta R_i. \tag{8.16}$$

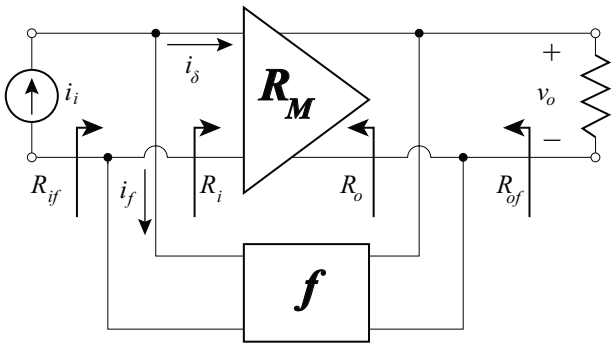


Figure 8.4: Input and output resistance for shunt-shunt feedback.

The two input currents, i_i and i_δ, are related through the forward gain and the feedback ratio:

$$i_\delta = i_i - i_f = i_i - i_\delta(R_M f) \quad \Rightarrow \quad i_i = i_\delta(1 + R_M f). \tag{8.17}$$

Therefore, combining Equations (8.15) and (8.17) yields:

$$R_{if} = \frac{v}{i_i} = \frac{v}{i_\delta(1 + R_M f)} = \frac{R_i}{1 + R_M f}. \tag{8.18}$$

The input resistance to feedback amplifier is the input resistance of the forward gain amplifier reduced by a factor of the return difference. *Shunt-series* feedback amplifier input resistance is similarly derived (replacing R_M by A_I). The same basic reduction in input resistance occurs:

$$R_{if} = \frac{R_i}{1 + A_I f}. \tag{8.19}$$

2. *Series mixing increases input resistance.* For the series-series feedback amplifier of Figure 8.5, the voltage across its input terminals v_i and the input current (arbitrarily identified as i), are related by the feedback amplifier input resistance, R_{if}:

$$v_i = iR_{if}. \tag{8.20}$$

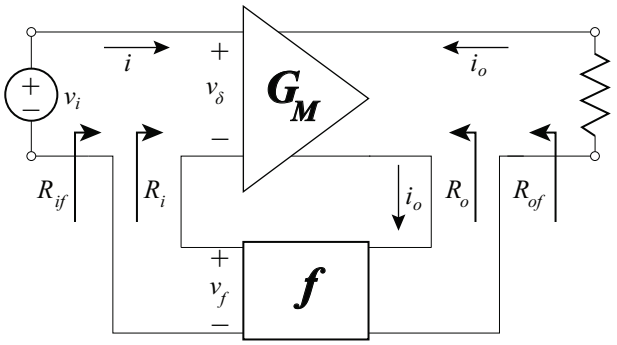


Figure 8.5: Input and output resistance for series-series feedback.

Similarly, the forward gain amplifier has input quantities related by its input impedance, R_i:

$$v_\delta = iR_i. \tag{8.21}$$

The two input voltages, v_i and v_δ , are related through the forward gain and the feedback ratio:

$$v_\delta = v_i - v_f = v_i - v_\delta(G_M f) \quad \Rightarrow \quad v_i = v_\delta(1 + G_M f). \tag{8.22}$$

Therefore, combining Equations (8.20) and (8.22) yields:

$$R_{if} = \frac{v_i}{i} = \frac{v_\delta(1 + G_M f)}{i} = R_i\,(1 + G_M f)\,. \tag{8.23}$$

The input resistance to feedback amplifier is the input resistance of the forward gain amplifier increased by a factor of the return difference. *Series-shunt* feedback amplifier input resistance is similarly derived (replacing G_M by A_V). The same basic increase in input resistance occurs:

$$R_{if} = R_i\,(1 + A_V f)\,. \tag{8.24}$$

It should be noted that resistors shunting the input, such as biasing resistors, often do not fit within the topological standards of series mixing. Thus, they must be considered separate from the feedback amplifier in order to properly model feedback amplifier characteristics using the techniques outlined in this, and following, chapters. Examples of such resistors will be found in the next section of this chapter.

The sampling process alters the output impedance of the feedback amplifier. Here shunt sampling decreases the output resistance and series sampling increases the output resistance.

1. *Shunt sampling decreases the output resistance.* For the *shunt-shunt* feedback amplifier of Figure 8.4, the output resistance is measured by applying a voltage source of value, v, to the output terminals with the input, i_i, set to zero value. A simplified schematic representation of that measurement is shown in Figure 8.6. In this figure, the forward-gain amplifier has been shown with its appropriate gain parameter, R_M, and output resistance, R_o.

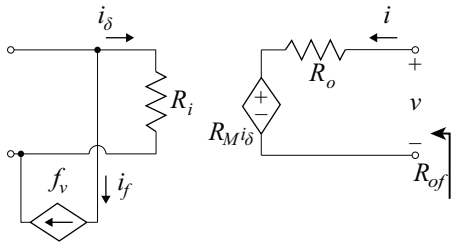


Figure 8.6: Schematic representation of shunt-shunt feedback for output resistance calculations.

The output resistance of the feedback system is the ratio,

$$R_{of} = \frac{v}{i}. \tag{8.25}$$

In the case where the input current has been set to zero,

$$i_\delta = -i_f = -f v. \tag{8.26}$$

Combining Equations (8.25) and (8.26) yields:

$$i = \frac{v - R_M(-f\, v)}{R_o} \quad \Rightarrow \quad R_{of} = \frac{v}{i} = \frac{R_o}{1 + R_M f}. \tag{8.27}$$

The output resistance of the feedback amplifier is the output resistance of the forward gain amplifier decreased by a factor of the return difference. *Series-shunt* feedback amplifier output resistance is similarly derived (replacing R_M by A_V). The same basic reduction in input resistance occurs:

$$R_{of} = \frac{R_o}{1 + A_V f}. \tag{8.28}$$

Resistors that shunt the output terminals, such as a load resistor, are considered as part of the feedback amplifier. The forward gain parameter (R_M or A_V) must be calculated in a consistent fashion with the consideration of these elements.

2. *Series sampling increases the output resistance.* For the *series-series* feedback amplifier of Figure 8.5, the output resistance is measured by applying a current source of value, i, to the output terminals with the input, v_i, set to zero value. A simplified schematic representation of that measurement is shown in Figure 8.7. In this figure, the forward-gain amplifier has been shown with its appropriate gain parameter, A_V, and output resistance, R_o.

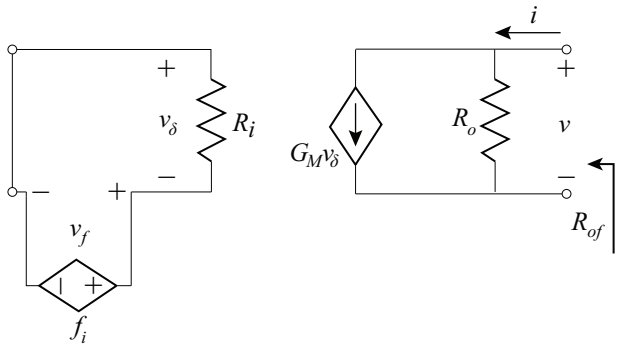


Figure 8.7: Schematic representation of series-series feedback for output resistance calculations.

The output resistance of the feedback system is the ratio,

$$R_{of} = \frac{v}{i}. \tag{8.29}$$

The voltage, v, is given by:

$$v = (i - G_M v_\delta) R_o. \tag{8.30}$$

Since the input voltage, v_i, has been set to zero value,

$$v_\delta = -v_f = -f_i. \tag{8.31}$$

Combining Equations (8.30) and (8.31) yields:

$$v = (i - G_M\{-f i\})R_o = i(1 + G_M f)R_o. \tag{8.32}$$

The output resistance is then given by:

$$R_{of} = \frac{v}{i} = (1 + G_M f)\ R_o. \tag{8.33}$$

The output resistance of the feedback amplifier is the output resistance of the forward gain amplifier increased by a factor of the return difference. *Shunt-series* feedback amplifier output resistance is similarly derived (replacing G_M by A_I). The same basic increase in input resistance occurs:

$$R_{of} = (1 + A_I f)\ R_o. \tag{8.34}$$

It should be noted that resistances shunting the output, such as load resistances, do not fit within the topological standards of series sampling. Thus, they must be considered separate from the feedback amplifier in order to properly model feedback amplifier characteristics using the techniques outlined in this, and following, chapters. The forward gain parameters, A_I and G_M, must be calculated excluding these resistances. Examples of such resistances will be found in the next section of this chapter.

Table 8.2: Summary of feedback amplifier resistance parameters[5]

	shunt-shunt	*shunt-series*	*series-shunt*	*series-series*
Input Resistance	$R_{if} = \dfrac{R_i}{1+R_M f}$	$R_{if} = \dfrac{R_i}{1+A_I f}$	$R_{if} = R_i(1+A_V f)$	$R_{if} = R_i(1+G_M f)$
Output Resistance	$R_{of} = \dfrac{R_o}{1+R_M f}$	$R_{of} = R_o(1+A_I f)$	$R_{of} = \dfrac{R_o}{1+A_V f}$	$R_{of} = R_o(1+G_M f)$

8.3 PRACTICAL FEEDBACK CONFIGURATIONS

Previous discussions of feedback and feedback configurations have been limited to idealized systems and amplifiers. The four idealized feedback schematic diagrams of Figure 8.3 identify the forward-gain amplifier and the feedback network as two-port networks with a very specific property: each is a device with one-way gain. Realistic electronic feedback amplifiers can only approximate that idealized behavior. In addition, in practical feedback amplifiers there is always some interaction between the forward-gain amplifier and the feedback network. This interaction most often takes the form of input and output resistive loading of the forward-gain amplifier. The division of the practical feedback amplifier into its forward-gain amplifier and feedback network is also not always obvious. These apparent obstacles to using idealized feedback analysis can be resolved through the use of two-port network relationships in the derivation of practical feedback amplifier properties. Once amplifier gain and impedance relationships have been derived, the utility of the two-port representations becomes minimal and is typically discarded.

Feedback topology is determined through careful observation of the interconnection of the feedback network and forward-gain amplifier. Shunt mixing occurs at the input terminal of the amplifier. Thus, *shunt mixing* is identified by a connection of feedback network and the forward-gain amplifier at the input terminal of first active device within the amplifier, that is:

[5]Series mixing feedback amplifiers that have resistors shunting the input require special care in the application of these formulas. Also, feedback amplifiers with series sampling and loads that shunt the output require similar care. See Section 8.3 for examples of proper calculations.

- at the base of a BJT for a common-emitter or common-collector first stage,
- at the emitter of a BJT for a common-base first stage,
- at the gate of a FET for a common-source or common-drain first stage, or
- at the source of a FET for a common-gate first stage.

Series mixing occurs in a loop that contains the input terminal of the forward-gain amplifier and the controlling port of the first active device. The controlling port of a BJT in the forward-active region is the base-emitter junction: a FET in the saturation region is controlled by the voltage across the gate-source input port. *Series mixing* is characterized by a circuit element which is *both* connected to the output *and* in series with the input voltage and the input port of the first active device.

Identification of the sampling is derived from direct observation of the connection of the output of the basic forward amplifier and the feedback network. Shunt sampling is typically characterized by a direct connection of the feedback network to the output node: series sampling implies a series connection of the amplifier output, the feedback network, and the load. Two tests performed at the feedback amplifier output can aid in the determination of sampling topology:

- If the feedback quantity vanishes for a short-circuit load, the output voltage must be the sampled quantity. Thus, *zero feedback for a short-circuit load* implies *shunt sampling*.
- If the feedback quantity vanishes for an open-circuit load, the output current must be the sampled quantity. Thus, *zero feedback for a open-circuit load* implies *series sampling*.

After the topological type has been identified, each amplifier must be transformed into a form that allows for the use of the idealized feedback formulations. This transformation includes modeling the amplifier and the feedback network with a particular two-port representation that facilitates combination of elements. Once the transformations are accomplished, the amplifier performance parameters are easily obtained using the methods previously outlined in this Chapter. The particular operations necessary to transform each of the four feedback amplifier topological types require separate discussion. The examples in this section demonstrate the typical interconnection of a basic forward amplifier and a feedback network for each feedback topology. While BJT amplifiers form the examples of this section, the general approach applies to all feedback amplifiers regardless of active device type.

8.3.1 SHUNT-SHUNT FEEDBACK

Figure 8.8 shows the small-signal model of a typical shunt-shunt feedback amplifier. In this representation, the forward-gain amplifier and the feedback network have been replaced by their equivalent y-parameter two-port network representations so that parallel parameters can be easily combined. A resistive load has been applied to the output port; and, since shunt-shunt feedback

amplifiers are transresistance amplifiers, a Norton equivalent source has been shown as the input. It should also be noted that the forward-gain parameter of each two-port, y_{21}, is the transadmittance.

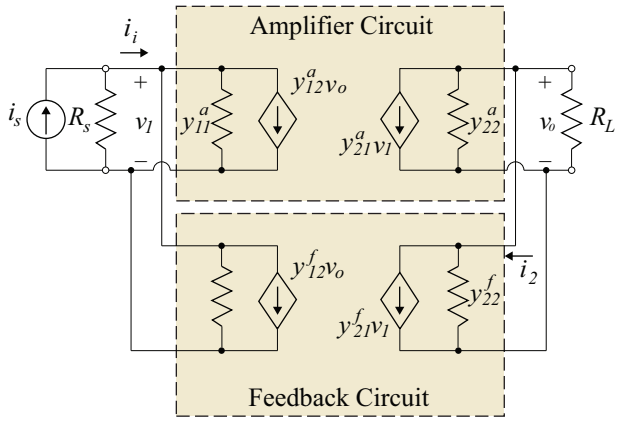


Figure 8.8: Two-port realization of a shunt-shunt feedback amplifier.

The basic feedback equation for a transresistance amplifier takes the form:

$$R_{Mf} = \frac{R_M}{1 + R_M f}. \tag{8.35}$$

The application of the basic feedback equation to this circuit in its current form is not immediately clear. It is necessary to transform the feedback amplifier circuit into a form that allows for easy application of the basic feedback equation, Equation (8.35). Such a transformation must meet the previously stated feedback requirements:

- The forward-gain amplifier is to be a forward transmission system only—its reverse transmission must be negligible.
- The feedback network is to be a reverse transmission system that presents a feedback current, dependent on the output voltage, to the amplifier input port.

While a mathematically rigorous derivation of the transformation is possible, greater insight to the process comes with a heuristic approach.

The two-port *y*-parameter representation, in conjunction with the shunt-shunt connection, is used to describe the two main elements of this feedback amplifier so that all the input port elements of both two-port networks are in parallel. Similarly, all output port elements are in parallel. It is well known that circuit elements in parallel may be rearranged and, so long as they remain in parallel, the circuit continues to function in an identical fashion. Hence, it is possible, *for analysis purposes only,* to *conceptually* move elements from one section of the circuit into another

(from the feedback circuit to the amplifier circuit or the reverse). The necessary conceptual changes made for the transformation are:

- The source resistance, the load resistance, and all input and output admittances, y_{11} and y_{22}, are placed in the modified amplifier circuit,[6]
- All forward transadmittances, y_{21}, (represented by current sources dependent on the input voltage, v_1) are placed in the modified amplifier circuit, and
- All reverse transadmittances, y_{12}, (represented by current sources dependent on the output voltage, v_o) are placed in the modified feedback circuit.

The dependent current source can be easily combined:

$$y_{12}^t = y_{12}^a + y_{12}^f, \tag{8.36}$$

and

$$y_{21}^t = y_{21}^a + y_{21}^f. \tag{8.37}$$

In virtually every practical feedback amplifier the reverse transadmittance of the forward-gain amplifier is much smaller than that of the feedback network ($y_{12}^a \ll y_{12}^f$) and the forward transadmittance of the feedback network is much smaller than that of the forward-gain amplifier ($y_{21}^f \ll y_{21}^a$). Thus, approximate simplifications of the amplifier representation can be made:

$$y_{12}^t = y_{12}^a + y_{12}^f \approx y_{12}^f, \tag{8.38}$$

and

$$y_{21}^t = y_{21}^f + y_{21}^a \approx y_{21}^a. \tag{8.39}$$

The shunt-shunt feedback amplifier circuit of Figure 8.8 is, with these changes and approximations, thereby transformed into the circuit shown in Figure 8.9.
This transformed circuit is composed of two simple elements:

- The original amplifier with its input shunted by the source resistance and the feedback network short-circuit input admittance, y_{11}^f, and its output shunted by the load resistance and the feedback network short-circuit output admittance, y_{22}^f.
- A feedback network composed solely of the feedback network reverse transadmittance, y_{12}^f.

[6]Inclusion of the source and load resistance in the amplifier seems, at first, counterproductive. It is necessary, however, to include these resistances so that the use of the feedback properties produces correct results for input and output resistance (after appropriate transformations).

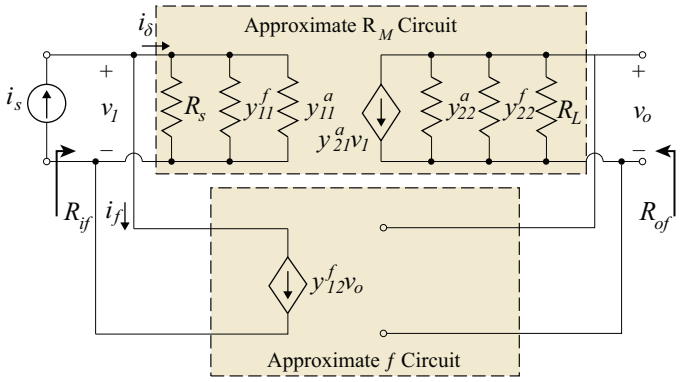


Figure 8.9: Redistributed shunt-shunt realization.

It is also important to notice that the input resistance, R_{if}, of this circuit includes the source resistance, R_s: as such *it is not the same as the input resistance of the true amplifier,* R_{in}. The input resistance of the true amplifier can be obtained as:

$$R_{in} = \left(\frac{1}{R_{if}} - \frac{1}{R_s} \right)^{-1}. \tag{8.40}$$

Similarly, the output resistance, R_{of}, of this circuit includes the load resistance, R_L: similar operations may be necessary to obtain the true output resistance of the amplifier.

The y-parameters of the feedback network can be obtained as outlined in Chapter 5:

$$y_{11}^f = \left. \frac{i_f}{v_1} \right|_{v_o=0}, \quad y_{22}^f = \left. \frac{i_2}{v_0} \right|_{v_1=0}, \quad \text{and} \quad y_{12}^f = \left. \frac{i_f}{v_0} \right|_{v_1=0}, \tag{8.41}$$

where i_2 is the current entering the output port of the feedback network (see Figure 8.8). With the determination of these two-port parameters, the circuit has been transformed into a form that is compatible with all previous discussions. The forward-gain parameter (in this case, R_M) of the loaded basic amplifier must be calculated, while the feedback ratio has been determined from the two-port analysis of the feedback network:

$$f = y_{12}^f. \tag{8.42}$$

In the case of totally resistive feedback networks, the shunting resistances can be found in a simple fashion:

- $r_{in} = (y_{11}^f)^{-1}$ is found by setting the output voltage to zero value, $v_o = 0$ and determining the resistance from the input port of the feedback network to ground.
- $r_{out} = (y_{22}^f)^{-1}$ is found by setting the input voltage to zero value, $v_i = 0$ and determining the resistance from the output port of the feedback network to ground.

The feedback ratio, f, is simply the ratio of the feedback current, i_f, to the output voltage when the input port of the feedback network, v_i, is set to zero value.

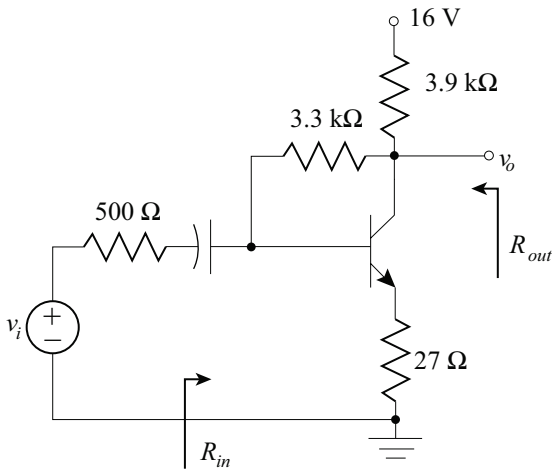
All idealized feedback methods can be applied to this transformed amplifier and all previously derived feedback results are valid.

Example 8.3

Determine the small-signal midband voltage gain,

$$A_{vf} = \frac{v_o}{v_i},$$

and the indicated input and output resistances for the feedback amplifier shown. The Silicon BJT is described by $\beta_F = 150$.



Solution::

This amplifier has typical shunt-shunt topology with a simple resistor as the feedback network. This resistor is directly connected to the base of the input of a common-emitter amplifier: this connection signifies shunt mixing. Similarly, the direct connection to the output node signifies shunt sampling (if the load is replaced by a short circuit, the feedback goes to zero). As outlined above, analysis of feedback amplifiers follows a distinct procedure:

DC Analysis:

As in all amplifier designs, the DC quiescent conditions must be determined so that the BJT h-parameters can be determined. The primary equation of interest for this amplifier is a loop equation passing through the DC source and the BJT base-emitter junction:

$$16 - 3.9\,\text{k}(151 I_B) - 3.3\,\text{k} I_B - 0.7 - 27(151 I_B) = 0.$$

This equation leads to the quiescent conditions:

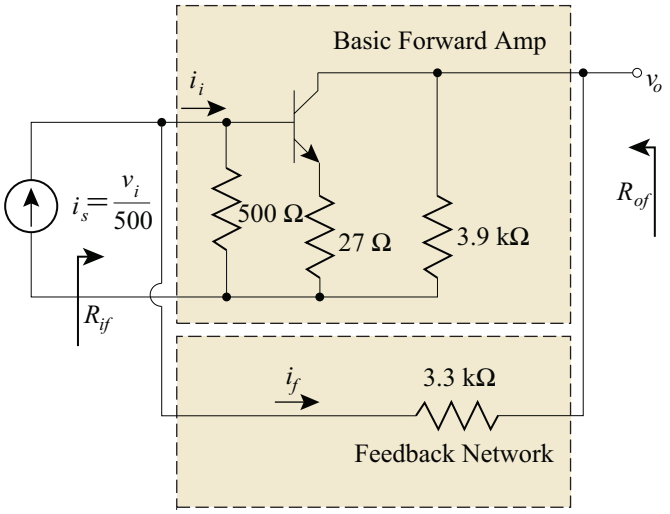
$$I_B = 25.66\,\mu\text{A}, \quad I_C = 3.849\,\text{mA}, \quad \text{and} \quad V_{CE} = 0.785\,\text{V}.$$

The significant BJT h-parameters are determined from these conditions to be:

$$h_{fe} = 150 \qquad h_{ie} = 1.020\,\text{k}\Omega\,.$$

Partition the Circuit into its Functional Modules:

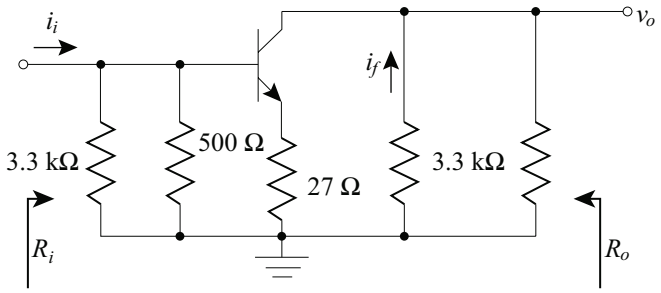
The AC equivalent amplifier circuit must be partitioned into its basic functional modules so that analysis can proceed. In addition a Norton equivalent of the source must be made so that the source resistance shunts the input. The functional modules necessary are: the basic forward amplifier, the feedback network, and the source. The load resistance and the output resistance of the source must be included in the basic forward amplifier module.



Load the Basic Forward Amplifier:

The input and output of the basic forward amplifier must be loaded with the short-circuit input and output admittances of the feedback network. That process is accomplished by: shunting the input with a duplicate of the feedback network whose output has been shorted; and shunting the output with a duplicate of the feedback network whose input has been shorted. The results of such operations are shown at the right. Notice that the feedback network resistances (in this case the 3.3 kΩ resistor) may appear in this loaded circuit more than once. After identifying the feedback current, i_f, on the output portion of the circuit, the feedback quantity, f, can also be determined from this circuit from the duplicate of the feedback network loading the output:

$$f = \left.\frac{i_f}{v_o}\right|_{v_i=0} = \frac{-1}{3.3\text{ k}}.$$



Loaded Basic Forward Amplifier

Determine the Performance of the Loaded Forward Amplifier:
The determination of the AC performance of the loaded forward amplifier follows the procedures that have been developed in previous chapters. The input resistance is given by:

$$R_i = 3.3\text{k}/500/\left\{h_{ie} + (1 + h_{fe})27\right\} = 434.2/\left\{1.02\text{k} + (1 + 150)27\right\} = 400.1\ \Omega.$$

The output resistance is:

$$R_o = 3.9\,\text{k}//3.3\,\text{k} = 1.788\,\text{k}\Omega.$$

The amplifier forward transresistance is given by:

$$R_M = \frac{v_o}{i_i} = \left(\frac{v_o}{v_i}\right)\left(\frac{v_i}{i_i}\right) = (A_V)\,(R_i)$$

$$R_M = \left(\frac{-150\{3.9\,\text{k}/3.3\,\text{k}\}}{\{1.020\,\text{k} + (1 + 150)27\}}\right)(400.12) = -21.05\,\text{k}\Omega.$$

Apply the Feedback Relationships to Obtain Total Circuit Performance:
All of the necessary quantities have been determined for the use of the feedback relationships.

$$D = 1 + Af = 1 + R_M f = 1 - 21.05\,\text{k}\left(\frac{-1}{3.3\,\text{k}}\right) = 7.3782$$

$$R_{if} = \frac{R_i}{D} = \frac{400,12}{7.3782} = 54.23\Omega \qquad R_{of} = \frac{R_o}{D} = \frac{1.7875}{7.7.3782} = 242.3\Omega$$

$$R_{Mf} = \frac{R_M}{D} = \frac{-21.05\,\text{k}}{7.3782} = -2.8525\,\text{k}\Omega.$$

The feedback circuit performance parameters are obtained through simple relationships. The voltage gain is obtained with the current/voltage relationship of a Norton/Thévenin transformation:

$$A_{Vf} = \left.\frac{v_o}{v_s}\right|_f = \left.\frac{v_o}{i_s}\right|_f \frac{i_s}{v_s} = R_{Mf}\left(\frac{1}{500}\right) = \frac{-2.8527\,\text{k}}{500} = -5.705 \approx -5.70.$$

The output resistance is as shown and does not require modification:

$$R_{out} = R_{of} \approx 242\,\Omega.$$

The input resistance must undergo the transformation of Equation (8.40):

$$R_{in} = \left(\frac{1}{R_{if}} - \frac{1}{500}\right)^{-1} = \left(\frac{1}{54.23} - \frac{1}{500}\right)^{-1} \approx 60.8\ \Omega.$$

It is helpful to reiterate the procedure for finding the performance parameters of a feedback amplifier. In order to find the feedback amplifier performance parameters, the following procedure is followed:

- Perform a DC analysis to obtain active device performance parameters
- Draw an AC equivalent circuit of the entire circuit
- Partition the circuit into its functional modules
- Load the Basic Forward Amplifier
- Determine the Performance of the Loaded Forward Amplifier.
- Apply the Feedback Relationships to Obtain Total Circuit Performance
- If necessary, transform these performance parameters into equivalent performance parameters as specified.

This procedure can be followed with all four feedback topologies in the same manner as has been shown in Example 8.3. The specifics of loading the basic forward amplifier and the application of the feedback formulas will vary according to the topology.

8.3.2 SHUNT-SERIES FEEDBACK

Figure 8.10 shows the small-signal model of a typical shunt-series feedback amplifier. In this representation, the forward-gain amplifier and the feedback network have been replaced by their equivalent g-parameter two-port network representations so that input and output parameters can be easily combined. A resistive load has been applied to the output port; and, since shunt-series feedback amplifiers are current amplifiers, a Norton equivalent source has been shown as the input. The forward-gain parameter of each two-port, g_{21}, is the voltage gain.
The basic feedback equation for a current amplifier takes the form:

$$A_{if} = \frac{A_I}{1 + A_I f}. \tag{8.43}$$

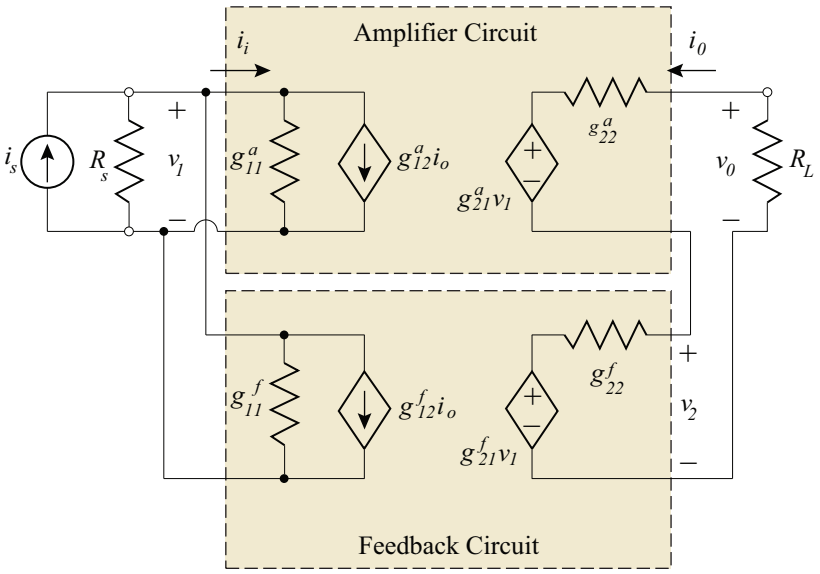


Figure 8.10: Two-port realization of a shunt-series feedback amplifier.

Once again, it is necessary to transform the feedback amplifier circuit into a form that allows for easy application of the basic feedback equation, Equation (8.43). Such a transformation must meet the previously stated feedback requirements:

- The forward-gain amplifier is to be a forward transmission system only—its reverse transmission must be negligible.
- The feedback network is to be a reverse transmission system that presents a feedback current, dependent on the output voltage, to the amplifier input port.

The two-port g-parameter representation, in conjunction with the shunt-series connection, is used to describe the two main elements of this feedback amplifier so that all the input port elements of both two-port networks are in parallel. In contrast, all output port elements are in series. *For analysis purposes only,* elements are *conceptually* moved elements from one section of the circuit into another (from the feedback circuit to the amplifier circuit or the reverse). The necessary conceptual changes made for the transformation are:

- The source resistance; all input admittances (g_{11}), and output impedances (g_{22}), are placed in the modified amplifier circuit. The load resistance is kept separate.
- All forward voltage gains (g_{21}) (represented by voltage sources dependent on the input voltage, v_1) are placed in the modified amplifier circuit, and

- All reverse current gains (g_{12}) (represented by current sources dependent on the output current, i_o) are placed in the modified feedback circuit.

The dependent current source can be easily combined:

$$g_{12}^t = g_{12}^a + g_{12}^f, \tag{8.44}$$

and

$$g_{21}^t = g_{21}^a + g_{21}^f. \tag{8.45}$$

In virtually every practical feedback amplifier the reverse current gain of the forward-gain amplifier is much smaller than that of the feedback network ($g_{12}^a \ll g_{12}^f$) and the forward voltage gain of the feedback network is much smaller than that of the forward-gain amplifier ($g_{21}^f \ll g_{21}^a$). Thus, approximate simplifications of the amplifier representation can be made:

$$g_{12}^t = g_{12}^a + g_{12}^f \approx g_{12}^f, \tag{8.46}$$

and

$$g_{21}^t = g_{21}^a + g_{21}^f \approx g_{21}^a. \tag{8.47}$$

The shunt-series feedback amplifier circuit of Figure 8.10 is, with these changes and approximations, thereby transformed into the circuit shown in Figure 8.11.

This transformed circuit is composed of two simple elements:

- The original amplifier with its input shunted by the source resistance and the feedback network open-circuit input admittance, g_{11}^f, and its output in series with the feedback network short-circuit output admittance, g_{22}^f and the load resistance.
- A feedback network composed solely of the feedback network reverse transadmittance, g_{12}^f.

As in the other case of shunt mixing, it is important to notice that the input resistance, R_{if}, of this circuit includes the source resistance, R_s: as such *it is not the same as the input resistance of the true amplifier,* R_{in}. The input resistance of the true amplifier can be obtained as:

$$R_{in} = \left(\frac{1}{R_{if}} - \frac{1}{R_s}\right)^{-1}. \tag{8.48}$$

The output resistance, R_{of}, of this circuit *does not include* the load resistance, R_L.

The g-parameters of the feedback network can be obtained as outlined in Chapter 5:

$$g_{11}^f = \left.\frac{i_f}{v_1}\right|_{i_o=0}, \qquad g_{22}^f = \left.\frac{v_2}{i_0}\right|_{v_1=0}, \qquad \text{and} \qquad g_{12}^f = \left.\frac{i_f}{i_0}\right|_{v_1=0}, \tag{8.49}$$

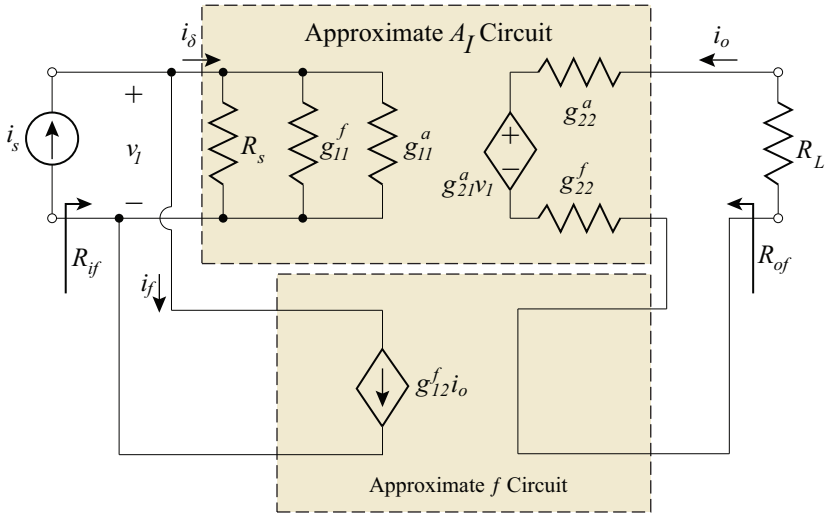


Figure 8.11: Redistributed shunt-series realization.

where v_2 is the voltage across the output port of the feedback network (see Figure 8.10). With the determination of these two-port parameters, the circuit has been transformed into a form that is compatible with all previous discussions. The forward-gain parameter (in this case, A_I) of the loaded basic amplifier must be calculated, while the feedback ratio has been determined from the two-port analysis of the feedback network:

$$f = g_{12}^f. \tag{8.50}$$

In the case of totally resistive feedback networks, the loading resistances can be found in a simple fashion:

- $r_{in} = \left(g_{11}^f\right)^{-1}$ is found by setting the output current to zero value, $i_o = 0$ and determining the resistance from the input port of the feedback network to ground. r_{in} shunts the input.
- $r_{out} = g_{22}^f$ is found by setting the input voltage to zero value, $v_i = 0$ and determining the resistance from the output port of the feedback network to ground. r_{out} is in series with the output.

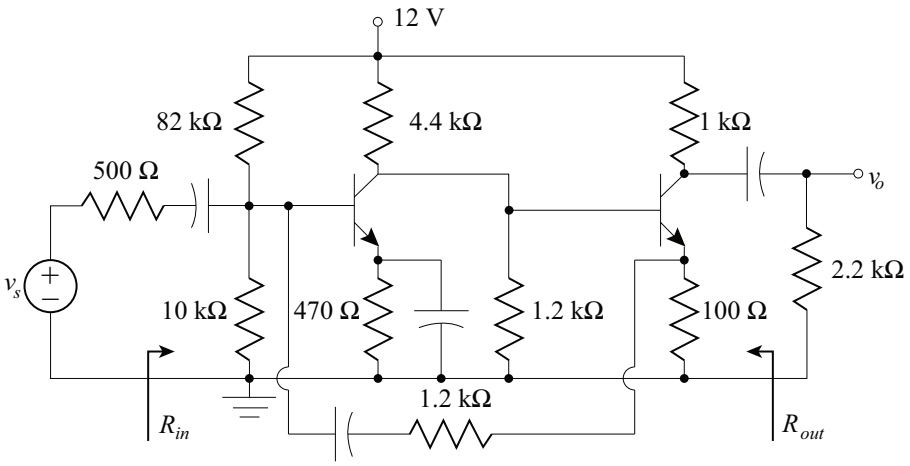
The feedback ratio, f, is simply the ratio of the feedback current, i_f, to the output current when the input port of the feedback network, v_i, is set to zero value.

Example 8.4

The circuit shown below is a shunt-series feedback amplifier. Determine the indicated input and output resistances and the midband voltage gain:

$$A_v = \frac{v_o}{v_s}.$$

The Silicon BJTs are described by $\beta_F = 150$.



Solution::

As in Example 8.3, the direct connection of the feedback network to the base of the input BJT signifies shunt mixing. At the output, however, the feedback is connected to the emitter of the output BJT, whereas the output is at the collector. Simple shorting of the output voltage has no effect on the feedback, while opening the collector of the output BJT eliminates all feedback: the sampling topology must be series sampling.

DC Analysis:

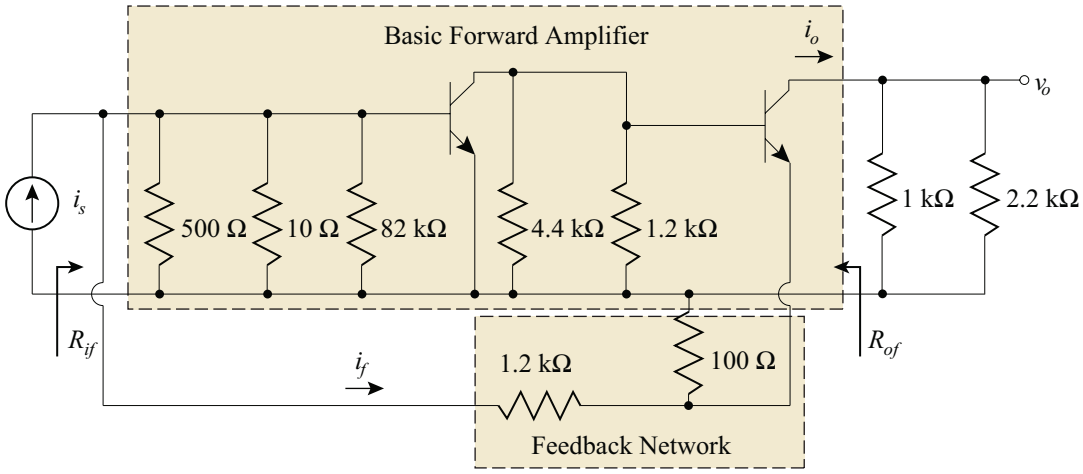
As in all amplifier designs, the DC quiescent conditions must be determined so that the BJT *h*-parameters can be determined. After setting all capacitors to open circuits, the usual analysis techniques lead to:

$$I_{c1} = 1.136\,\text{mA} \quad \Rightarrow \quad h_{ie1} = 3.46\,\text{k}\Omega$$
$$I_{c2} = 7.494\,\text{mA} \quad \Rightarrow \quad h_{ie2} = 524\,\Omega.$$

Partition the Circuit into its Functional Modules:

The AC equivalent amplifier circuit must be partitioned into its basic functional modules so that analysis can proceed. In addition a Norton equivalent of the source must be made so that the

source resistance shunts the input. The functional modules necessary are: the basic forward amplifier, the feedback network, the source, and the load. The output resistance of the source must be included in the basic forward amplifier module.

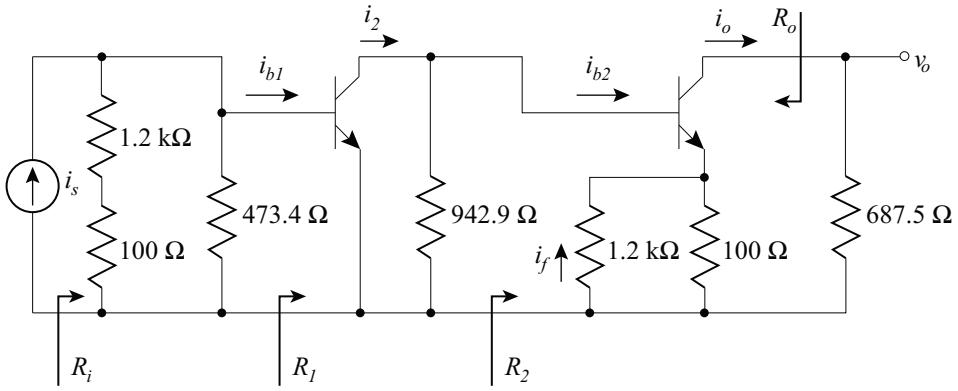


Replacing the source with its Norton equivalent gives to the relationship:

$$i_s = \frac{v_s}{500}.$$

Load the Basic Forward Amplifier:

The basic forward amplifier must have its input and output ports loaded. The input port is shunted with the feedback network whose output port has been open-circuited (shown as a series connection of 1.2 kΩ and 100 Ω). The output must have the feedback network, with its input port shorted to ground, placed in series with the output current (here at the emitter of the output BJT). This basic loading is shown above. Resistors in parallel (from the partitioned circuit) have been combined in order to simplify later calculations.



In addition, the feedback ratio, f, is easily determined from the output loading circuit. The feedback current is identified in the output circuit (feedback current is *subtracted* from the input, thus it flows *toward* the output port) and a ratio is formed:

$$f = \frac{i_f}{i_o} = \left(\frac{i_f}{i_{e2}}\right)\left(\frac{i_{e2}}{i_o}\right) = \left(\frac{100}{100 + 1.2\,\text{k}}\right)\left(\frac{151}{150}\right) = 0.07744.$$

Determine the Performance of the Loaded Forward Amplifier:

The input resistance of each amplifier stage is calculated:

$$R_1 = h_{ie1} = 3.46\,\text{k}\Omega$$
$$R_2 = h_{ie2} + 151(1.2\,\text{k}//100) = 14.46\,\text{k}\Omega.$$

The input resistance of the basic loaded amplifier is given by:

$$R_i = 1.3\,\text{k}//473.4//R_1 = 315.4\,\Omega.$$

The current gain can be calculated as:

$$A_I = \left(\frac{i_o}{i_s}\right) = \left(\frac{i_o}{i_{b2}}\right)\left(\frac{i_{b2}}{i_2}\right)\left(\frac{i_2}{i_{b1}}\right)\left(\frac{i_{b1}}{i_s}\right)$$
$$A_I = (150)\left(\frac{942.9}{942.9 + 14.46\,\text{k}}\right)(150)\left(\frac{1.3\,\text{k}//473.4}{1.3\,\text{k}//473.4 + 3.46\,\text{k}}\right) = 125.6.$$

The output resistance is approximately infinite.

Apply the Feedback Relationships to Obtain Total Circuit Performance:

With the calculation of the input and output resistance, the current gain, and the feedback ratio, it becomes possible to use the feedback relationships to find circuit performance including the effects of both the loading and feedback.

$$D = 1 + A_{If} = 1 + 125.6(0.07744) = 10.72$$
$$A_{If} = \frac{A_I}{D} = \frac{125.6}{10.72} = 11.71$$
$$R_{if} = \frac{R_i}{D} = \frac{315.4}{10.72} = 29.42 \qquad R_{of} \approx \infty.$$

The defined performance characteristics are altered forms of the above relationships:

$$A_{Vf} = \left.\frac{v_o}{v_s}\right|_f = \left(\frac{v_o}{i_o}\right)\left(\left.\frac{i_o}{i_s}\right|_f\right)\left(\frac{i_s}{v_s}\right) = (1\,\text{k}//2.2\,\text{k})\,(11.71)\left(\frac{1}{500}\right) = 16.1$$
$$R_{in} = \left(\frac{1}{R_{if}} - \frac{1}{R_s}\right)^{-1} = 31.3\ \Omega \qquad R_{out} = R_{of}//1\,\text{k} = 1\,\text{k}\Omega.$$

8.3.3 SERIES-SHUNT FEEDBACK

Figure 8.12 is the small-signal model of a typical series-shunt feedback amplifier. In this representation, the forward-gain amplifier and the feedback network have been replaced by their equivalent h-parameter two-port network representations. A resistive load has been applied to the output port; and, since series-shunt feedback amplifiers are voltage amplifiers, a Thévenin equivalent source has been shown as the input. The forward-gain parameter of each two-port, h_{21}, is the current gain.

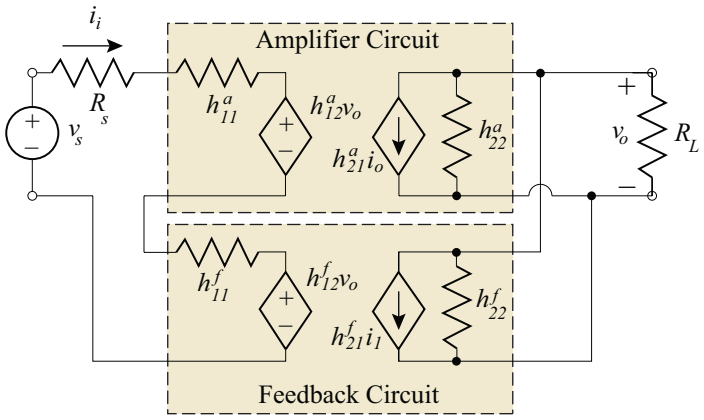


Figure 8.12: Two-port realization of a series-shunt feedback amplifier.

The basic feedback equation for a voltage amplifier takes the form:

$$A_{Vf} = \frac{A_V}{1 + A_V f}. \tag{8.51}$$

Again a transformation of the circuit is necessary. The two-port h-parameter representation, in conjunction with the series-shunt connection, is used to describe the two main elements of this feedback amplifier so that all the input port elements of both two-port networks are in series. All output port elements are in parallel. *For analysis purposes only,* elements are *conceptually* moved from one section of the circuit into another:

- The load resistance all input impedances (h_{11}) and all output admittances (h_{22}) are placed in the modified amplifier circuit,
- All forward current gains, h_{21}, (represented by current sources dependent on the input current, i_i) are placed in the modified amplifier circuit, and
- All reverse voltage gains, h_{12}, (represented by voltage sources dependent on the output voltage, v_o) are placed in the modified feedback circuit.

The usual combinations and approximations hold:

$$h_{12}^t = h_{12}^a + h_{12}^f \approx h_{12}^f, \tag{8.52}$$

and

$$h_{21}^t = h_{21}^a + h_{21}^f \approx h_{21}^a. \tag{8.53}$$

The series-shunt feedback amplifier circuit of Figure 8.12 is, with these changes and approximations, thereby transformed into the circuit shown in Figure 8.13.

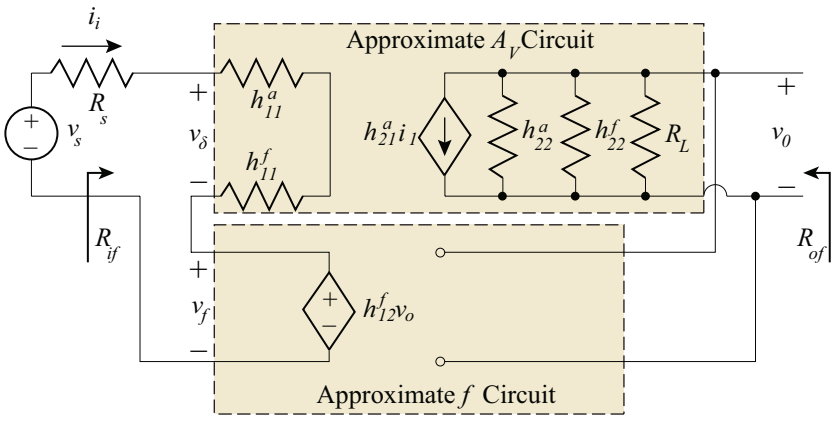


Figure 8.13: Redistributed series-shunt realization.

This transformed circuit is composed of two simple elements:

- The original amplifier with its output shunted by the load resistance and the feedback network open-circuit output admittance, h_{22}^f, and its input in series with the feedback network short-circuit input admittance, h_{11}^f and the source resistance.
- A feedback network composed solely of the feedback network reverse voltage gain, h_{12}^f.

It is important to notice that the output resistance, R_{of}, of this circuit includes the load resistance, R_L: as such *it may not the same as the output resistance of the true amplifier,* R_{out}. If the load resistance is not included in R_{out}, the correct expression is:

$$R_{out} = \left(\frac{1}{R_{of}} - \frac{1}{R_L} \right)^{-1}. \tag{8.54}$$

The input resistance, R_{if}, of this circuit *does not include* the source resistance, R_s or any other resistances in series with the input of the basic forward amplifier.

The h-parameters of the feedback network can be obtained as outlined in Chapter 5:

$$h_{11}^f = \left.\frac{v_1}{i_f}\right|_{v_o=0}, \quad h_{22}^f = \left.\frac{i_2}{v_0}\right|_{i_1=0}, \qquad \text{and} \qquad h_{12}^f = \left.\frac{v_f}{v_0}\right|_{i_1=0}, \tag{8.55}$$

where i_1 is the current entering the input port of the feedback network (see Figure 8.13). With the determination of these two-port parameters, the circuit has been transformed into a form that is compatible with all previous discussions. The forward-gain parameter (in this case, A_V) of the loaded basic amplifier must be calculated, while the feedback ratio has been determined from the two-port analysis of the feedback network:

$$f = h_{12}^f. \tag{8.56}$$

In the case of totally resistive feedback networks, the loading resistances can be found in a simple fashion:

- $r_{in} = h_{11}^f$ is found by setting the output voltage to zero value, $v_o = 0$ and determining the resistance from the input port of the feedback network to ground. r_{in} is in series with the input.

- $r_{out} = \left(h_{22}^f\right)^{-1}$ is found by setting the input current to zero value, $i_1 = 0$ and determining the resistance from the output port of the feedback network to ground. r_{out} shunts the output.

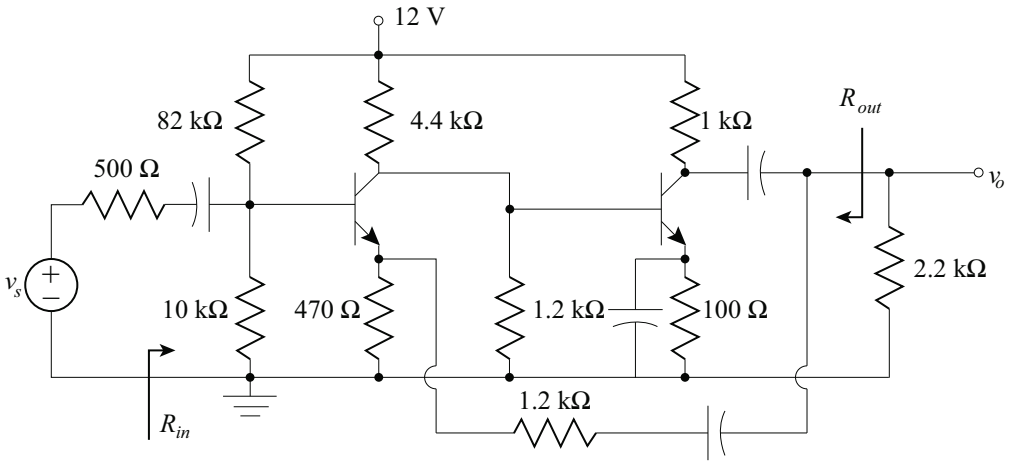
The feedback ratio, f, is simply the ratio of the feedback voltage, v_f, to the output voltage when the input current of the feedback network, i_1, is set to zero value.

Example 8.5

For the circuit shown, determine the indicated input and output resistances and the midband voltage gain,

$$A_v = \frac{v_o}{v_s}.$$

The Silicon BJTs are described by $\beta_F = 150$.



Solution::

In this circuit the feedback network is connected at the emitter of the input BJT. Feedback in the form of a voltage will appear here in series with a Thévenin source and the base-emitter junction of the BJT: this is series mixing. The direct connection of the feedback network to the output node implies shunt sampling (replacing the load with a short eliminates all feedback).

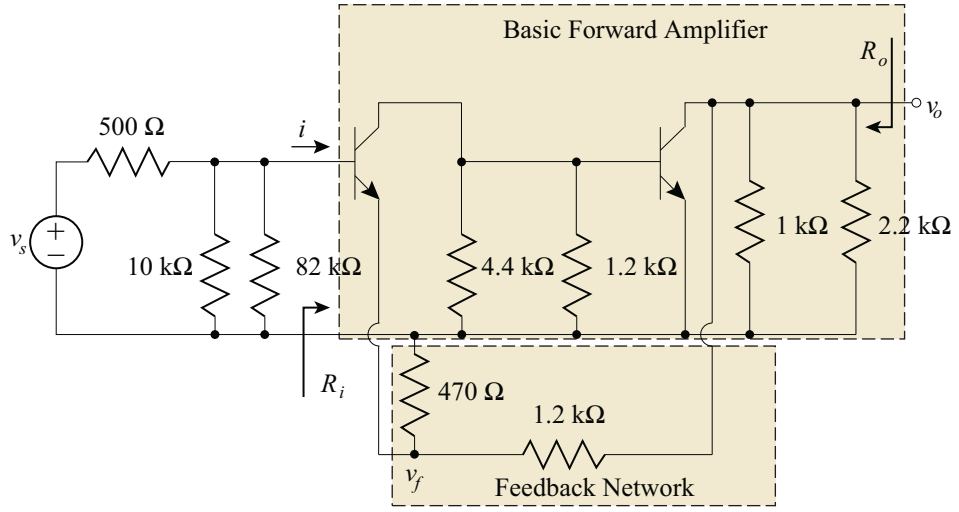
DC Analysis:

The DC portion of this circuit is identical to that of Example 8.4. The only changes have been in the feedback (which is capacitively coupled) and the resistors bypassed by capacitors. Thus, the DC quiescent conditions of the BJTs remain unchanged. The h-parameters are also the same as in Example 8.4:

$$h_{ie1} = 3.46\,\text{k}\Omega \qquad h_{ie2} = 524\,\Omega\,.$$

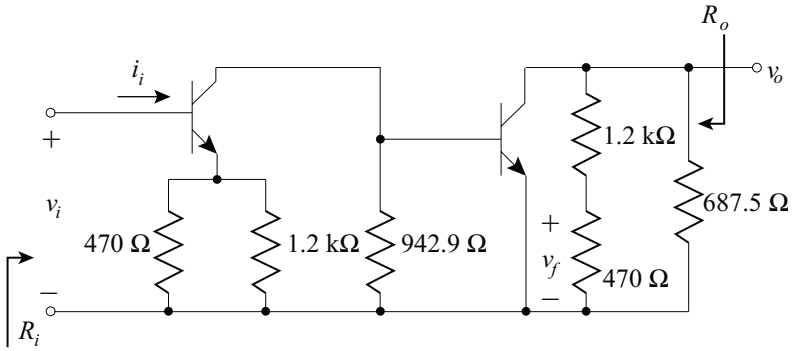
Partition the Circuit into its Functional Modules:

The AC equivalent amplifier circuit must be partitioned into its basic functional modules so that analysis can proceed. The functional modules necessary are: the basic forward amplifier, the feedback network, and the source. Of particular interest is that the bias resistors at the input of the first BJT must be partitioned within the source. This partitioning is due to the requirement of series mixing that items at the input must be in series. The load resistance is included in the basic forward amplifier module.



Load the Basic Forward Amplifier:

The basic forward amplifier must have its input and output ports loaded. The output port is shunted with the feedback network whose input port has been open-circuited (shown as a series connection of 1.2 kΩ and 470 Ω). The input must have the feedback network, with its output port shorted to ground, placed in series with the input active device (shown as the parallel connection 1.2 kΩ and 470 Ω in series with the emitter of the BJT). This basic loading is shown above. Resistors in parallel (from the partitioned circuit) have been combined in order to simplify later calculations.



In addition, the feedback ratio, f, is easily determined from the output loading circuit. The feedback voltage is identified on the output loading circuit (feedback voltage is *subtracted* from the input, thus its positive pole is toward the output port) and a ratio is formed:

$$f = \frac{v_f}{v_o} = \frac{470}{470 + 1.2\,\text{k}} = 0.2814.$$

Determine the Performance of the Loaded Forward Amplifier:
The input and output resistance of the loaded amplifier are calculated to be:

$$R_i = h_{ie1} + 151(470//1.2\,\text{k}) = 54.46\,\text{k}\Omega,$$

and

$$R_o = 687.5//1.67\,\text{k} = 487.0\,\Omega.$$

The voltage gain is given by:

$$A_V = \left(\frac{v_o}{v_i}\right) = \left(\frac{v_o}{v_1}\right)\left(\frac{v_1}{v_i}\right) = \left(\frac{-150(487.0)}{524}\right)\left(\frac{-150(942.9//524)}{54.46\,\text{k}}\right) = 129.4.$$

Apply the Feedback Relationships to Obtain Total Circuit Performance:
All necessary components are now available to use the feedback formulas:

$$D = 1 + A_{Vf} = 37.40 \qquad A_{Vf} = \frac{A_V}{D} = 3.46$$
$$R_{if} = R_i D = 2.037\,\text{M}\Omega \qquad R_{of} = \frac{R_o}{D} = 13.02\,\Omega.$$

In order to match the performance parameter definitions of the stated problem there must be a few alterations:

$$R_{in} = R_{if}//10\,\text{k}//82\,\text{k} = 8.87\,\text{k}\Omega \qquad R_{out} = \left(\frac{1}{R_{of}} - \frac{1}{2.2\,\text{k}}\right)^{-1} = 13.1\ \Omega$$
$$A_V = \frac{v_o}{v_s} = \left(\frac{v_o}{v_i}\right)\left(\frac{v_i}{v_s}\right) = A_{Vf}\left(\frac{R_{in}}{R_{in} + 500}\right) = 3.27.$$

8.3.4 SERIES-SERIES FEEDBACK

Figure 8.8 shows the small-signal model of a typical series-series feedback amplifier. In this representation, the forward-gain amplifier and the feedback network have been replaced by their equivalent z-parameter two-port network representations. A resistive load has been applied to the output port; and, since series-series feedback amplifiers are transconductance amplifiers, a Thévenin equivalent source has been shown as the input. The forward-gain parameter of each two-port, z_{21}, is the transimpedance.
The basic feedback equation for a transconductance amplifier takes the form:

$$G_{Mf} = \frac{G_M}{1 + G_M\, f}. \tag{8.57}$$

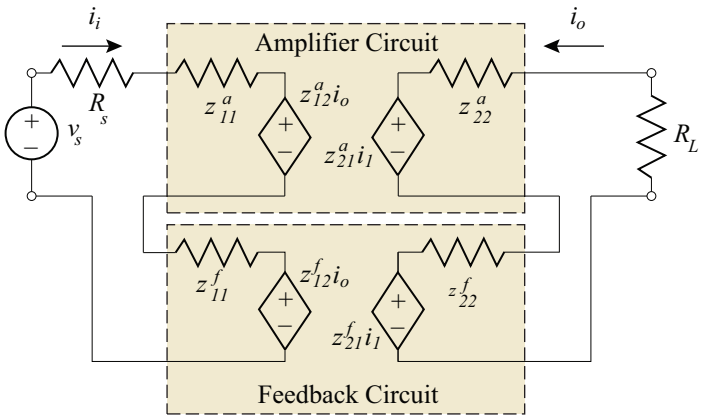


Figure 8.14: Two-port realization of a series-series feedback amplifier.

Again a transformation of the circuit is necessary. The two-port z-parameter representation, in conjunction with the series-series connection, is used to describe the two main elements of this feedback amplifier so that all the input port elements of both two-port networks are in series. All output port elements are in also in series. *For analysis purposes only,* elements are *conceptually* moved from one section of the circuit into another:

- The input and output impedances, z_{11} and z_{22}, are placed in the modified amplifier circuit,
- All forward transresistance, z_{21}, (represented by voltage sources dependent on the input current, i_1) are placed in the modified amplifier circuit, and
- All reverse transresistance, z_{12}, (represented by voltage sources dependent on the output current, i_o) are placed in the modified feedback circuit.

The usual combinations and approximations hold:

$$z^t_{12} = z^a_{12} + z^f_{12} \approx z^f_{12}, \tag{8.58}$$

and

$$z^t_{21} = z^a_{21} + z^f_{21} \approx z^a_{21}. \tag{8.59}$$

The series-series feedback amplifier circuit of Figure 8.14 is, with these changes and approximations, thereby transformed into the circuit shown in Figure 8.15.
This transformed circuit is composed of two simple elements:

- The original amplifier with its input in series with the feedback network short-circuit input impedance, z^f_{11} and the source resistance and its output in series with the feedback network short-circuit output impedance z^f_{22}, and the load.

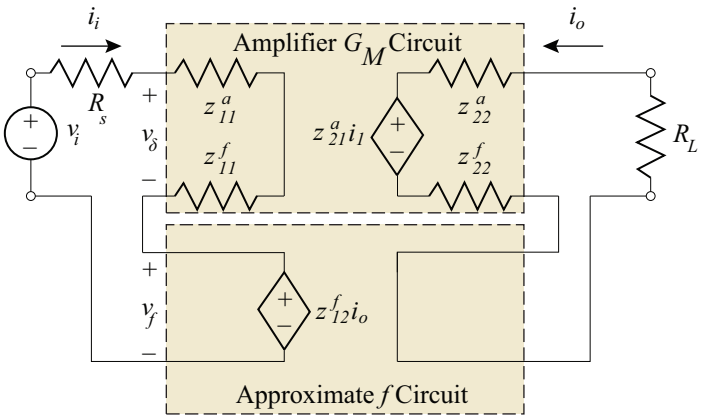


Figure 8.15: Redistributed series-series realization.

- A feedback network composed solely of the feedback network reverse transresistance, z_{12}^f.

The z-parameters of the feedback network can be obtained as outlined in Chapter 5:

$$z_{11}^f = \left.\frac{v_1}{i_1}\right|_{i_o=0}, \quad z_{22}^f = \left.\frac{v_0}{i_o}\right|_{i_1=0}, \quad \text{and} \quad z_{12}^f = \left.\frac{v_f}{i_0}\right|_{i_1=0}, \tag{8.60}$$

where i_1 is the current entering the input port of the feedback network (see Figure 8.14). With the determination of these two-port parameters, the circuit has been transformed into a form that is compatible with all previous discussions. The forward-gain parameter (in this case, G_M) of the loaded basic amplifier must be calculated, while the feedback ratio is determined from the two-port analysis of the feedback network:

$$f = z_{12}^f. \tag{8.61}$$

In the case of totally resistive feedback networks, the loading resistances can be found in a simple fashion:

- $r_{in} = z_{11}^f$ is found by setting the output current to zero value, $i_o = 0$ and determining the resistance from the input port of the feedback network to ground. r_{in} is in series with the input.
- $r_{out} = z_{22}^f$ is found by setting the input current to zero value, $i_1 = 0$ and determining the resistance from the output port of the feedback network to ground. r_{out} is in series with the output.

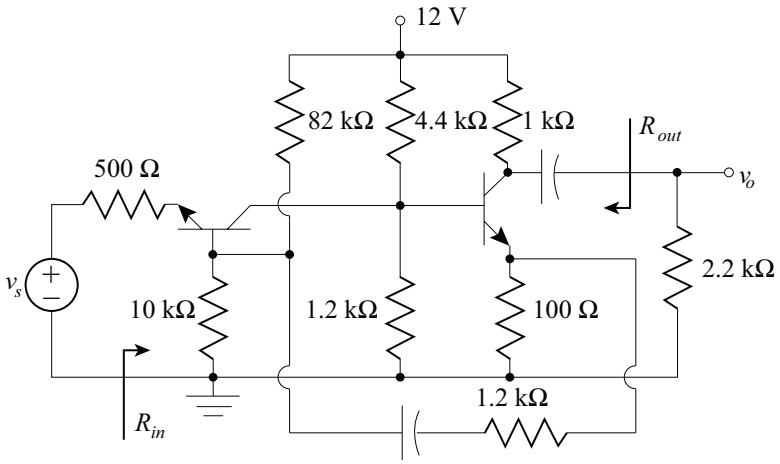
The feedback ratio, f, is simply the ratio of the feedback voltage, v_f, to the output current when the input current of the feedback network, i_1, is set to zero value.

Example 8.6

Determine the following midband performance parameters for the circuit shown: The indicted input and output resistances and voltage gain:

$$A_v = \frac{v_o}{v_s}.$$

The transistors are silicon with parameters $\beta_F = 150$.



Solution::

In this circuit, the feedback network is connected to the base of the input BJT, but the input is at the emitter. Again, feedback will appear in series with the input and the base-emitter junction of the BJT: this is series mixing. The connection of the feedback network at the output characterizes series sampling (opening *both* load resistors at the collector of the output BJT eliminated all feedback).

DC Analysis:

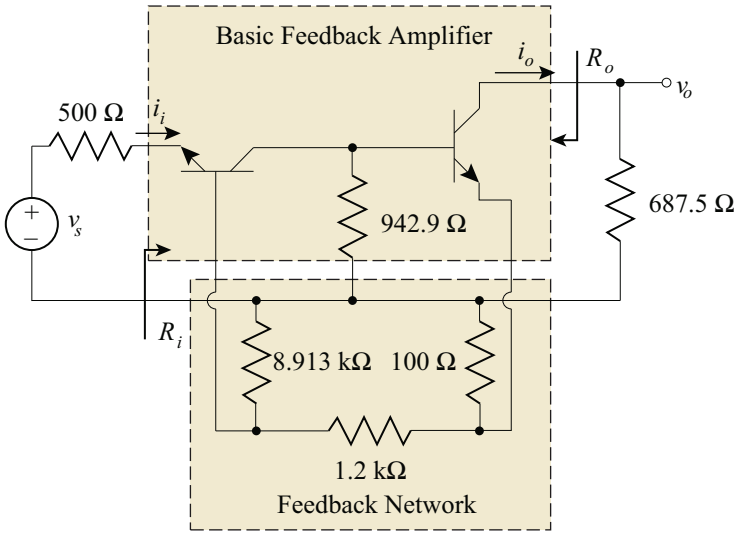
As in all amplifier designs, the DC quiescent conditions must be determined so that the BJT *h*-parameters can be determined. After setting all capacitors to open circuits, the usual analysis techniques lead to:

$$I_{c1} = 1.074\,\text{mA} \quad \Rightarrow \quad h_{ie1} = 3.66\,\text{k}\Omega$$
$$I_{c2} = 8.030\,\text{mA} \quad \Rightarrow \quad h_{ie2} = 489\,\Omega.$$

Partition the Circuit into its Functional Modules:

The amplifier is partitioned into its two functional modules. Series mixing implies the need for a Thévenin source. Since there is series mixing at both input and output port, the source and load resistances are excluded from the basic forward amplifier.

The AC model of the partitioned amplifier is shown below with all parallel resistances combined.

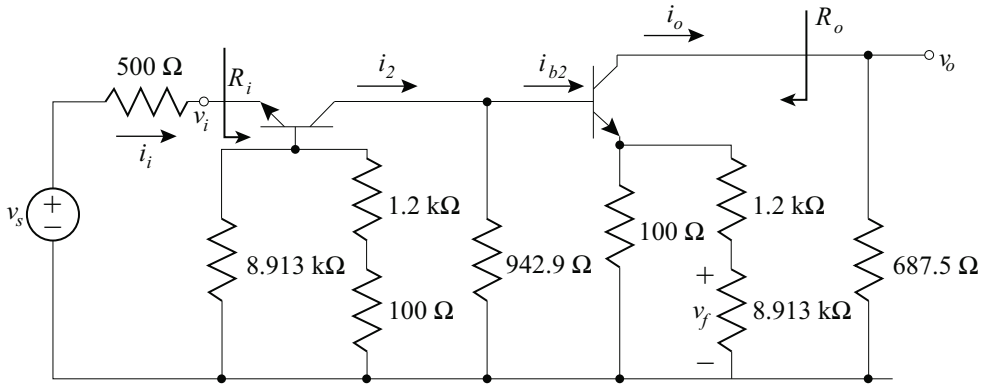


Load the Basic Forward Amplifier:

The input loading is achieved by setting the output current, i_o, to zero value. This opens the output port of the feedback network and forms the input loading circuit connected to the base of the input BJT. The output loading is achieved by setting the input current, i_i, to zero value. This opens the input port of the feedback network and forms the output loading circuit connected to the emitter of the output BJT.

The feedback quantity, v_f, is then drawn on the output loading circuit (positive end toward the load). The feedback ratio is determined to be:

$$f = \frac{v_f}{i_o} = \left(\frac{-151}{150}\right)\left(\frac{100}{100 + 1.2\,\text{k} + 8.913\,\text{k}}\right)(8.913\,\text{k}) = -87.85\Omega\,.$$



Determine the Performance of the Loaded Forward Amplifier:

The following relationships can be determined for the loaded basic forward amplifier. The input resistance to the total circuit is given by the input resistance of a common-base amplifier:

$$R_i = \frac{h_{ie1} + R_b}{h_{fe} + 1} = \frac{3.66\,\text{k} + (8.913\,\text{k}//1.3\,\text{k})}{151} = 31.72\,\Omega.$$

The input resistance to the common emitter stage is given by:

$$R_{i1} = h_{ie2} + 151\,(100//\,(1.2\,\text{k} + 8.913\,\text{k})) = 15.441\,\text{k}\Omega.$$

With these two relationships, the forward transconductance can be calculated:

$$G_M = \frac{i_o}{v_i} = \left(\frac{i_o}{i_{b2}}\right)\left(\frac{i_{b2}}{i_2}\right)\left(\frac{i_2}{i_i}\right)\left(\frac{i_i}{v_i}\right) = (-150)\left(\frac{942.9}{942.9 + R_{i2}}\right)\left(\frac{150}{151}\right)\left(\frac{1}{R_i}\right) = -0.2703\,\text{S}.$$

The output resistance of this amplifier is approximately infinite.

Apply the Feedback Relationships to Obtain Total Circuit Performance:

With the forward-gain, feedback ratio, input resistance and output resistance calculated for the basic loaded forward amplifier. The effects of feedback can now be easily calculated:

$$D = 1 + G_{Mf} = 1 + (-0.2703)(-87.85) = 24.75$$
$$R_{if} = R_i D = 785 \qquad R_{of} = R_o D \approx \infty$$
$$G_{Mf} = \frac{G_M}{D} = -0.010923.$$

These results are then transformed into the proper performance parameters as defined in the statement of the problem:

$$A_{Vf} = \left.\frac{v_o}{v_s}\right|_f = \left(\frac{v_o}{i_o}\right)\left(\left.\frac{i_o}{v_i}\right|_f\right)\left(\left.\frac{v_i}{v_s}\right|_f\right) = (1\,\text{k}//2.2\,\text{k})\,(G_{Mf})\left(\frac{R_{if}}{R_{if} + 500}\right) = -4.59,$$

$$R_{in} = R_{if} = 785\,\Omega \qquad R_{out} = R_{of}//1\,\text{k} = 1\,\text{k}\Omega\,.$$

8.4 CONCLUDING REMARKS

The fundamental advantages of the use of feedback in electronic amplifiers have been described in this chapter. Reduction in non-linear distortion, variation in amplifier performance parameters, and control of input and out impedance are all significant benefits available through the use of feedback.

The analysis of feedback amplifiers can be a complex process complicated by the interaction of the basic forward amplifier and the feedback network. It is, however, possible to simplify this analysis process through the use of a few basic feedback relationships and a systematic analysis method. This analysis method consists of a seven step process:

- Identify the Feedback Topology
- Perform a DC Analysis to Obtain Active Device Performance Parameters
- Partition the AC Equivalent Circuit into its Functional Modules
- Load the Basic Forward Amplifier
- Determine the Performance of the Loaded Forward Amplifier
- Apply the Feedback Relationships to Obtain Total Circuit Performance
- If Necessary, Transform these Performance Parameters into Equivalent Performance Parameters as Specified.

Vital to the analysis method are the partitioning of the circuit into its functional modules and loading the basic forward amplifier. Table 8.3 serves as an aid in that process, itemizing the process variation due to feedback topology.

Another significant benefit of feedback, the increase in the midband frequency range, will be extensively discussed in Chapter 11 (Book 3).

Summary Design Example

The design process often involves the modification of an existing design to meet new, but similar, performance specifications. As an example, the feedback amplifier shown below constructed with enhancement-mode FETs with the following properties:

$$K = 1\,\text{mA/V} \qquad V_T = 1.5\,\text{V} \qquad V_A = 160\,\text{V}.$$

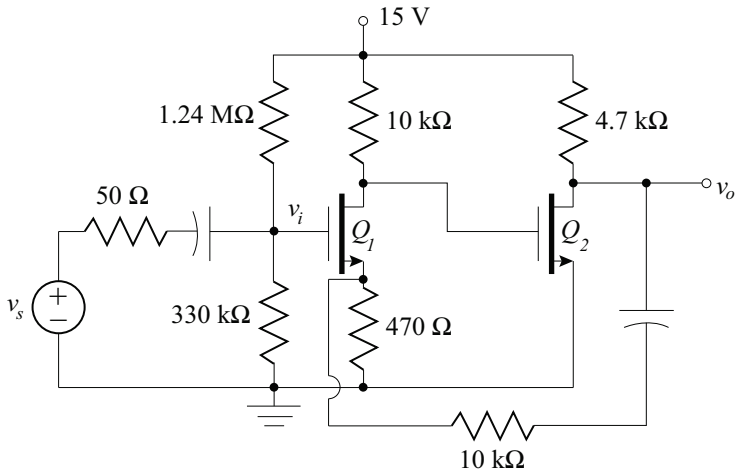
Table 8.3: Feedback amplifier analysis

	Topology			
	shunt-shunt	***shunt-series***	***series-shunt***	***series-series***
input X_i	current, i_s	current, i_s	voltage, v_s	voltage, v_s
output X_o	voltage, v_o	current, i_o	voltage, v_o	current, i_o
Signal Source	Norton	Norton	Thévenin	Thévenin
Input Circuit	Include Shunt Resistances; Set $v_o = 0$	Include Shunt Resistances; Set $i_o = 0$	Exclude Shunt Resistances; Set $v_o = 0$	Exclude Shunt Resistances; Set $i_o = 0$
Output Circuit	Include Shunt Resistances; Set $v_i = 0$	Exclude Shunt Resistances; Set $v_i = 0$	Include Shunt Resistances; Set $i_i = 0$	Exclude Shunt Resistances; Set $i_i = 0$
feedback ratio f	i_f / v_o	i_f / i_o	v_f / v_o	v_f / i_o
forward gain A	transresistance R_M	current gain A_I	voltage gain A_V	transconductance G_M
Input Resistance	$R_{if} = \dfrac{R_i}{1 + R_M f}$	$R_{if} = \dfrac{R_i}{1 + A_I f}$	$R_{if} = R_i (1 + A_V f)$	$R_{if} = R_i (1 + G_M f)$
Output Resistance	$R_{of} = \dfrac{R_o}{1 + R_M f}$	$R_{of} = R_o (1 + A_I f)$	$R_{of} = \dfrac{R_o}{1 + A_V f}$	$R_{of} = R_o (1 + G_M f)$

Notes:

Input/Output Circuit: These procedures give the basic forward amplifier without feedback but including the effects of loading due to the feedback network.

Resistance: Resistance: the resistance modified at shunted ports will include all shunting resistances that were included in the basic forward amplifier. The resistance modified at series ports will only include the resistances included in the basic forward amplifier. The true amplifier input and output impedance must be modified to reflect the point of measurement desired.



This amplifier is known to have the to have high input resistance ($\approx 260\,\text{k}\Omega$), moderate output resistance ($\approx 300\,\Omega$), and a midband voltage gain:

$$A = \frac{v_o}{v_s} \approx 18.3.$$

The quiescent conditions for the transistors are known to be:

$$I_{D1} = 1.19\,\text{mA} \qquad \text{and} \qquad I_{D2} = 2.47\,\text{mA}.$$

It is desired to design an amplifier with similar input and output resistance and a midband voltage gain of 15. Redesign the amplifier to meet the new design goals.

Solution:

If at all possible, a redesign process should minimize the number of changes. For the given amplifier, the FET AC parameters will remain the same if the quiescent drain currents are not changed. Thus, it seems advantageous to retain the same Q-poing. This proposed redesign constraint limits changes to the feedback resistor ($10\,\text{k}\Omega$) and the load resistor ($4.7\,\text{k}\Omega$). While variation in either will alter the maximum symmetrical output swing, voltage gain is more strongly dependent on the feedback resistor: less variation in quiescent output voltage will result in changing the feedback resistor. It is therefore decided to alter *only the feedback resistor* to accomplish the new design goals.

This amplifier is a series-shunt feedback amplifier: the gain parameter that is stabilized is the voltage gain from the input port to the output port. In order to meet the new design goals the gain with feedback must be (the input resistance of this amplifier simply is the parallel combination of the bias resistors and *does not change* with variation in feedback):

$$A_{vf} = A = \frac{R_{in}}{R_{in} + 50} = 15.0029.$$

The expression for the *loaded gain* of the amplifier *without feedback* is given by:

$$A_v = \left(\frac{-g_{m1} r_{d1}(10\,\text{k})}{r_{d1} + 10\,\text{k} + g_{m1} r_{d1}(470//R_f)} \right) \left(-g_{m2} \left[r_{d2}//4.7\,\text{k}//(470 + R_f) \right] \right).$$

The feedback quantity is given by:

$$f = \frac{v_f}{v_o} = \frac{470}{470 + R_f}.$$

If the quiescent condition do not change with the redesign, the FET parameters can easily be found to be:

$$g_m = 2\sqrt{I_D K} \quad \Rightarrow \quad g_{m1} = 2.18\,\text{mA/V}, \quad g_{m2} = 3.14\,\text{mA/V}$$
$$r_d = \frac{V_A}{I_D} \quad \Rightarrow \quad r_{d1} = 134\,\text{k}\Omega, \quad r_{d2} = 64.8\,\text{k}\Omega.$$

Thus, for the original design the gain is given by:

$$A_v = (-10.6)(-9.7) = 102.8 \quad f = 0.04489 \quad A_{vf} = 18.31.$$

Two alternatives exist for finding the value of R_f so that the design goals are met:

- a mathematical search of the exact gain expression
- reasonable approximations of the gain expression

In this case, neither provides a significant advantage in the trade off between difficulty and accuracy of the result. A mathematical search provides $R_f = 7.882\,\text{k}\Omega$. One reasonable set of approximations are shown below.

In the expression for A_v, the parallel combination of R_f with $470\,\Omega$ is unlikely to change significantly with reasonable variation in R_f. A good approximation to the unloaded gain is therefore:

$$A_v = (-10.6) \left(-g_{m2} \left[r_{d2}//4.7\,\text{k}// \left(470 + R_f \right) \right] \right) = 0.03328 \left[4.382\,\text{k}// \left(470 + R_f \right) \right].$$

The gain with feedback can then be written as:

$$A_{vf} = \frac{0.03328 \left\{ \dfrac{4.382\,\text{k}(470 + R_f)}{4.382\,\text{k} + (470 + R_f)} \right\}}{1 + 0.03328 \left\{ \dfrac{4.382\,\text{k}(470 + R_f)}{4.382\,\text{k} + (470 + R_f)} \right\} \left\{ \dfrac{470}{(470 + R_f)} \right\}}.$$

Significant cancellation occurs:

$$A_{vf} = \frac{0.03328 \left\{ 4.382\,\text{k}(470 + R_f) \right\}}{4.382\,\text{k} + (470 + R_f) + 0.03328 \left\{ 4.382\,\text{k} \right\} \left\{ 470 \right\}}.$$

This expression can easily be solved for R_f so that the gain $A_{vf} = 15.0029$:

$$R_f = \frac{A_{vf}\,(4.382\,\text{k} + 0.03328\,(4.382\,\text{k})\,(470))}{0.03328\,\{4.382\,\text{k}\} - A_{vf}} - 470 = 7.892\ \text{k}\Omega.$$

The variation between this approximate solution and the exact solution is 0.127%. The closest standard value resistor is 7.87 kΩ.

Redesign summary:

The original circuit remains essentially the same with the exception that the feedback resistor is reduced in value from 10 kΩ to 7.87 kΩ.

8.5 PROBLEMS

8.1. The voltage gain of an amplifier is subject to a variation given by

$$A = 238 \pm 4\,\text{V/V}.$$

It is desired to use this amplifier as the fundamental forward-gain element in a feedback amplifier. The feedback amplifier must have no more than 0.15% variation in its voltage gain.

(a) Determine the necessary feedback ratio to achieve this variation while achieving maximum gain.

(b) What is the gain of the feedback amplifier?

8.2. An amplifier with an open-loop voltage gain $A_V = 1000 \pm 100$ is given. The amplifier must be altered so that the voltage gain varies by no more than 0.5%.

(a) Find the feedback factor, f, to achieve this variation while achieving maximum gain.

(b) Find the gain of the feedback amplifier.

8.3. A feedback amplifier must be designed to have a closed-loop voltage gain of 120 utilizing a feedback network with an feedback factor $f = 0.02$. Determine the range of values of the gain, A_V, for which the closed-loop gain, A_{Vf}, is:

(a) 120 ± 1

(b) 120 ± 0.2

8.4. Design a feedback amplifier that has a nominal gain of 200 with no more than 1% variation in overall gain due to the variation of individual elements. The individual elements available are amplifier stages having a gain of 2000 with 25% variation. Other constraints require that feedback be applied *only to each individual stage* and that such stages be connected in cascade.

8.5. Design a feedback amplifier that has a nominal gain of 200 with no more than 1% variation in overall gain due to the variation of individual elements. The individual elements available are amplifier stages having a gain of 2000 with 25% variation. Other constraints require that stages be connected in cascade and that feedback be applied *only to the total cascade-connected amplifier.*

8.6. The gain of an amplifier is described by the relationship:

$$A(v) = 10 \left| atan\left(\frac{v}{4}\right)\right| + 5,$$

for input voltages ranging from $-10\,\text{V}$ to $+10\,\text{V}$. Feedback is applied to the circuit so that the feedback ratio, $f = 0.1$

(a) Plot the voltage transfer relationship of the original amplifier.

(b) On the same graph, plot the voltage transfer relationship of the feedback amplifier.

(c) Quantitatively, compare the linearity of the feedback amplifier to that of the amplifier without feedback. Comment on results.

8.7. The gain of an amplifier is described by the relationship:

$$A(v) = 10 \left| atan\left(\frac{v}{4}\right)\right| + 5.$$

(a) Determine the input, v, necessary to produce an output of value, 50.

(b) If a sinusoid of the amplitude, v (determined in part (a)), is the input to this amplifier, what is the total harmonic distortion of the output?

(c) Feedback is applied to the circuit so that the feedback ratio, $f = 0.1$. What value of the input to the new amplifier will produce an output of 50?

(d) Repeat part b with an input of amplitude, v, as determined in part (c). Compare results.

8.8. The gain of an amplifier is described by the relationship:

$$A(v) = \frac{v^2}{10} + \frac{v}{2} + 4,$$

for input voltages ranging from $-5\,\text{V}$ to $+5\,\text{V}$. Feedback is applied to the circuit so that the feedback ratio, $f = 0.6$

(a) Plot the voltage transfer relationship of the original amplifier.

(b) On the same graph, plot the voltage transfer relationship of the feedback amplifier.

(c) Quantitatively, compare the linearity of the feedback amplifier to that of the amplifier without feedback. Comment on results.

8.9. The gain of an amplifier is described by the relationship:

$$A(v) = \frac{v^2}{10} + \frac{v}{2} + 4,$$

(a) Determine the input, v, necessary to produce an output of value, 20.

(b) If a sinusoid of the amplitude, v (determined in part (a)), is the input to this amplifier, what is the total harmonic distortion of the output?

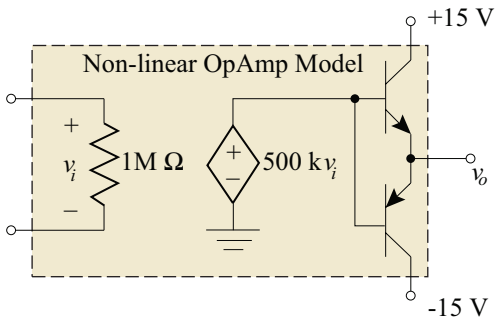
(c) Feedback is applied to the circuit so that the feedback ratio, $f = 0.6$. What value of the input to the new amplifier will produce an output of 20?

(d) Repeat part b with an input of amplitude, v, as determined in part (c). Compare results.

8.10. Despite the prominent crossover distortion inherent in Class B amplifiers, several OpAmp types use a Class B output stage. A simple model for such an OpAmp is shown. The application of feedback in the form of resistors connecting the input and output OpAmp terminals significantly reduces the crossover distortion so that the OpAmp can be used as an effective circuit element that is essentially linear.

(a) Determine the amplitude of an input sinusoidal voltage, v_i, that will produce a 1 V amplitude output for the circuit shown. Determine the total harmonic distortion of the output using SPICE (either with a .FOUR or .DISTO statement). Assume the OpAmp is loaded with a 470 Ω resistor and the BJTs are Silicon with $\beta_F = 75$.

(b) Design an OpAmp inverting amplifier with a voltage gain of 10 using the given OpAmp model and appropriate resistors. Using SPICE, apply a 0.1 V sinusoid to this amplifier (loaded with a 470 Ω resistor) and determine the total harmonic distortion of the output. Compare results to those obtained in part (a).

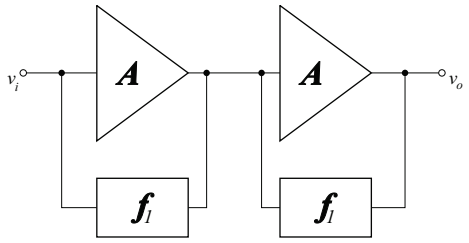


8.11. It is not intuitively obvious as to whether local or global feedback is most beneficial in a multistage amplifier. The two amplifiers shown are examples of each for a two-stage

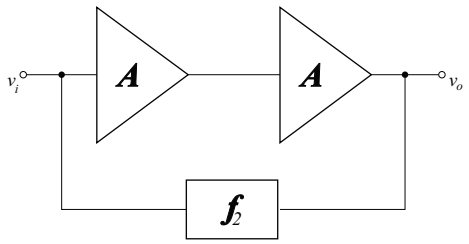
amplifier. The two feedback ratios, f_1 and f_2, are chosen so that the total gain, A_f, of each circuit is identical. The total gain includes all feedback effects and is defined as:

$$A_f = \frac{v_o}{v_i}.$$

Investigate which feedback amplifier configuration has greater resistance in the total gain, A_f, to variation in the gain of the individual stages, A.

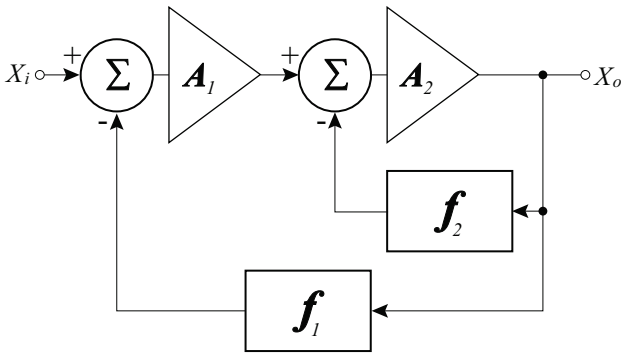


Local Feedback



Global Feedback

8.12. Complex amplifiers may incorporate both local and global feedback. The amplifier shown is an example of such a complex amplifier. Derive the transfer characteristic for this amplifier.



8.13. The BJT in the shunt-shunt feedback amplifier of Example 8.3 is replace by a BJT described by $\beta_F = 120$.

(a) Determine the change in the small-signal midband gain of the amplifier due to this substitution.

(b) Verify the gain with SPICE simulation

(c) Verify that the gain variation is within that predicted by the gain stabilization formulas.

8.14. The shunt-shunt feedback amplifier of Example 8.3 is to be redesigned to have a small-signal midband gain of:

$$A_{vf} = \frac{v_o}{v_i} = -6.0 \pm 0.05.$$

This change is to be accomplished by *alteration of the value of the feedback resistor only.*

(a) Determine the new resistance value that will meet the gain specifications.

(b) Determine the change in the input resistance due to the change.

(c) Verify results using SPICE.

8.15. For the single stage amplifier shown, the FET parameters are:

$$K = 1\,\text{mA/V}^2, \quad V_T = 1.5\,\text{V}, \quad \text{and} \quad V_A = 160\,\text{V}.$$

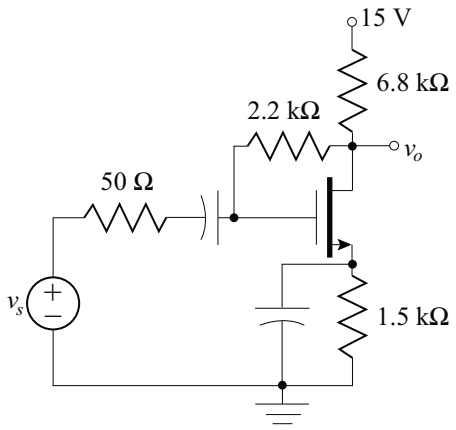
The FET is replaced by another described by:

$$K = 1.2\,\text{mA/V}^2, \quad V_T = 1.6\,\text{V}, \quad \text{and} \quad V_A = 150\,\text{V}.$$

(a) Determine the change in the small-signal midband gain of the amplifier due to this substitution.

$$A = \frac{v_o}{v_s}.$$

(b) Verify that the gain variation is within that predicted by the gain stabilization formulas.

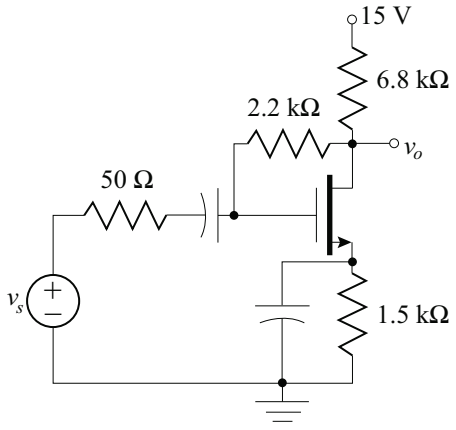


8.16. The design goal for the given feedback amplifier is a voltage gain

$$A = \frac{v_o}{v_s} = -5.$$

Redesign the amplifier to achieve that voltage gain goal. The FET is described by:

$$K = 1.2\,\text{mA/V}^2, \quad V_T = 1.6\,\text{V}, \quad \text{and} \quad V_A = 150\,\text{V}.$$



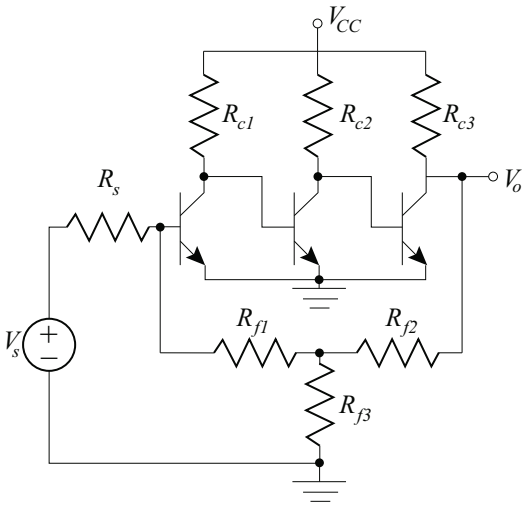
8.17. For the circuit shown, assume the transistors are biased into the forward-active region.

(a) Identify the topology of the feedback.

(b) Draw a circuit diagram of the loaded basic forward amplifier.

(c) Write the expression for the feedback ratio, f.

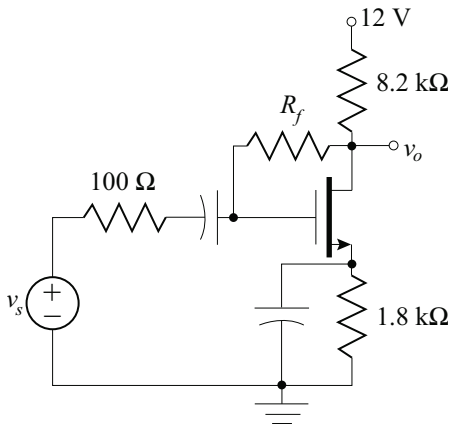
(d) Write the expression for the midband voltage gain in terms of the circuit and BJT parameters.



8.18. For the single stage amplifier shown, determine the value of R_f to achieve an overall midband voltage gain of magnitude 8.

The FET parameters are:

$$K = 1\,\text{mA/V}^2, \quad V_T = 1.5\,\text{V}, \quad \text{and} \quad V_A = 160\,\text{V}.$$

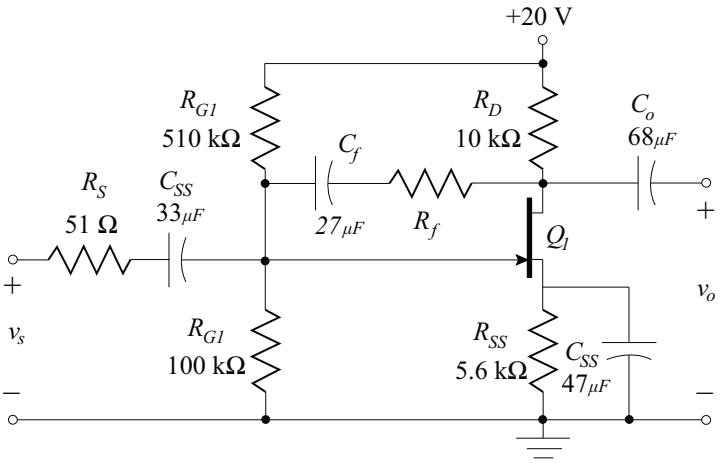


8.19. Complete the design of the circuit shown to achieve a closed-loop gain

$$A_{Vf} = -10.$$

The JFET characteristic parameters are:

$$V_{PO} = -3.5\,\text{V}, \quad I_{DSS} = 8\,\text{mA}, \quad \text{and} \quad V_A = 120\,\text{V}.$$

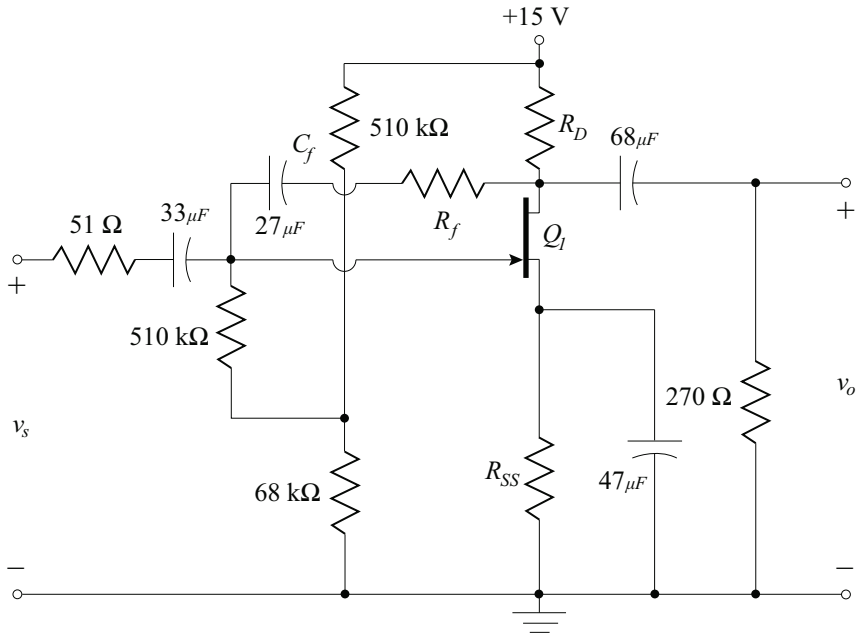


8.20. Complete the design of the circuit shown for a closed-loop gain $A_{Vf} = -10$. The JFET characteristic parameters are:

$$V_{PO} = -4\,\text{V}, \quad I_{DSS} = 8\,\text{mA}, \quad \text{and} \quad V_A = 120\,\text{V}.$$

The JFET is to be biased such that:

$$V_{GS} = -1\,\text{V} \quad \text{and} \quad V_{DS} = 7\,\text{V}.$$



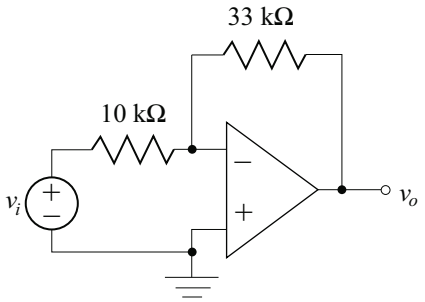
8.21. The performance parameters of the given OpAmp circuit can be determined using feedback techniques. The characteristics of the OpAmp are:

input resistance	1 MΩ
output resistance	75 Ω
voltage gain	500 kV/V

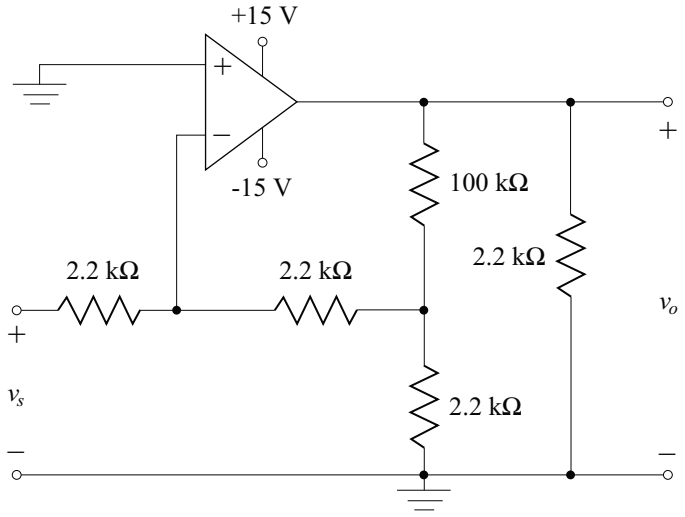
(a) Identify the feedback topology

(b) Draw a circuit diagram for the loaded basic forward amplifier.

(c) Determine the voltage gain for the total circuit using feedback techniques. Compare results to those determined using the techniques described in Chapter 1 (Book 1).



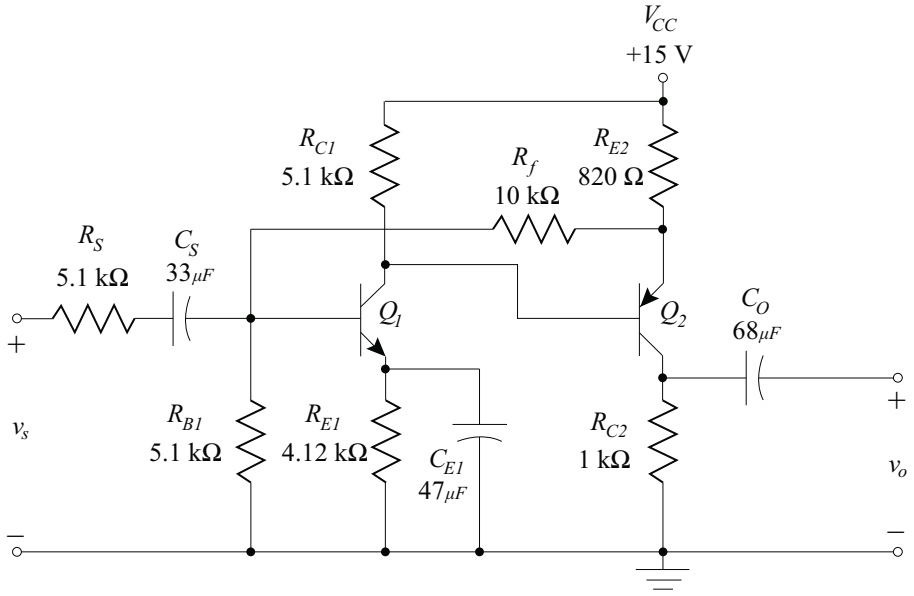
8.22. Use the principles of feedback analysis to find the closed-loop voltage gain, the input resistance R'_{if}, and output resistance R'_{of}. The OpAmp open-loop gain is $A_V = 10\,\text{kV/V}$, input resistance of the OpAmp is 1 MΩ, and the output resistance of the OpAmp is 75 Ω.



8.23. Determine the closed-loop gain, input resistance, and output resistance of the amplifier shown below. The transistors have the following characteristics:

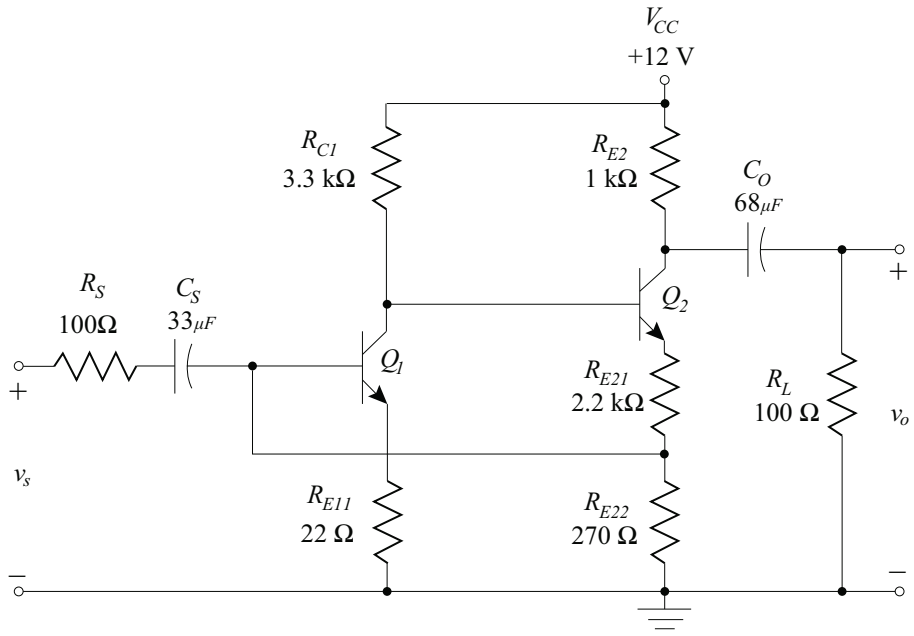
npn: $\beta_F = 200$, and $V_A = 120\,\text{V}$

pnp: $\beta_F = 200$, and $V_A = 100\,\text{V}$



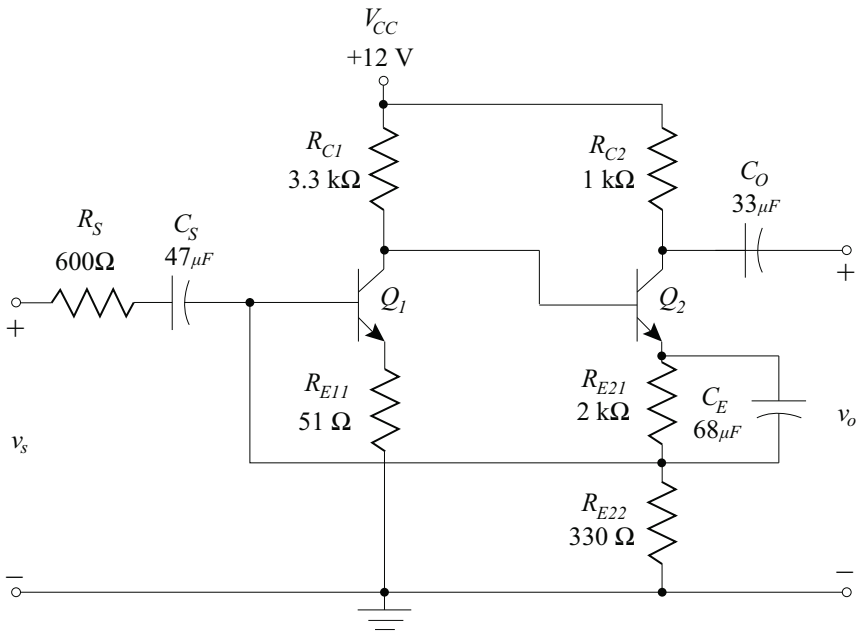
8.24. Determine the closed-loop gain, input resistance, and output resistance of the amplifier shown below. The transistors are identical and have the following characteristic parameters:

$$\beta_F = 200 \quad \text{and} \quad V_A = 120\,\text{V}.$$



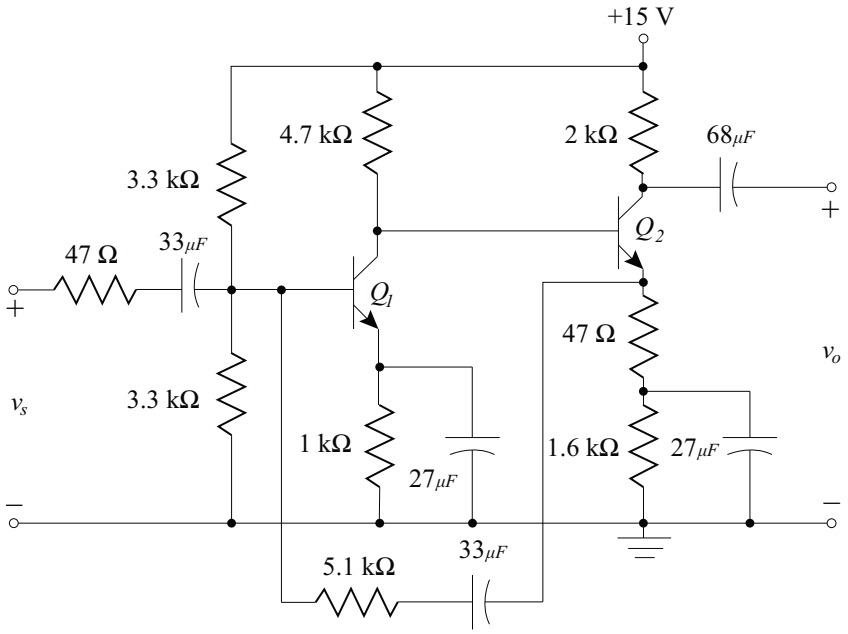
8.25. Determine the closed-loop gain, input resistance (not including the source resistor, R_S), and output resistance of the amplifier shown below. The transistors are identical and have the following characteristics:

$$\beta_F = 180 \quad \text{and} \quad V_A = 200\,\text{V}.$$



8.26. Determine the closed-loop gain, input resistance (not including the source resistor, R_S), and output resistance of the amplifier shown below. The transistors are identical and have the following characteristic parameters:

$$\beta_F = 200 \quad \text{and} \quad V_A = 120\,\text{V}.$$



8.27. The shunt-series feedback amplifier of Example 8.4 is to be redesigned to have a voltage gain:

$$A_v = \frac{v_o}{v_s} = 20 \pm 0.1.$$

The change is to be accomplished by alteration of the feedback (1.2 kΩ) resistor only. Complete this redesign and determine the effect of the change on input and output resistance of the amplifier. Use SPICE to verify the redesigned amplifier performance.

8.28. In an attempt to create a circuit with a midband voltage gain,

$$A_v = \frac{v_o}{v_s},$$

of twenty (20), the circuit shown was created.

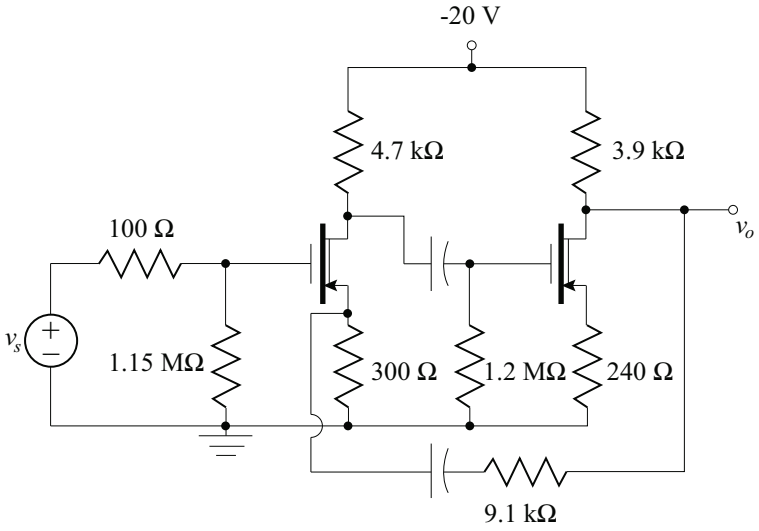
The *p*-channel MOSFET transistors have parameters,

$$V_{PO} = 2\,\text{V}, \quad I_{DSS} = -5\,\text{mA} \quad \text{and} \quad V_A = 200\,\text{V}.$$

(a) Identify the circuit topology.

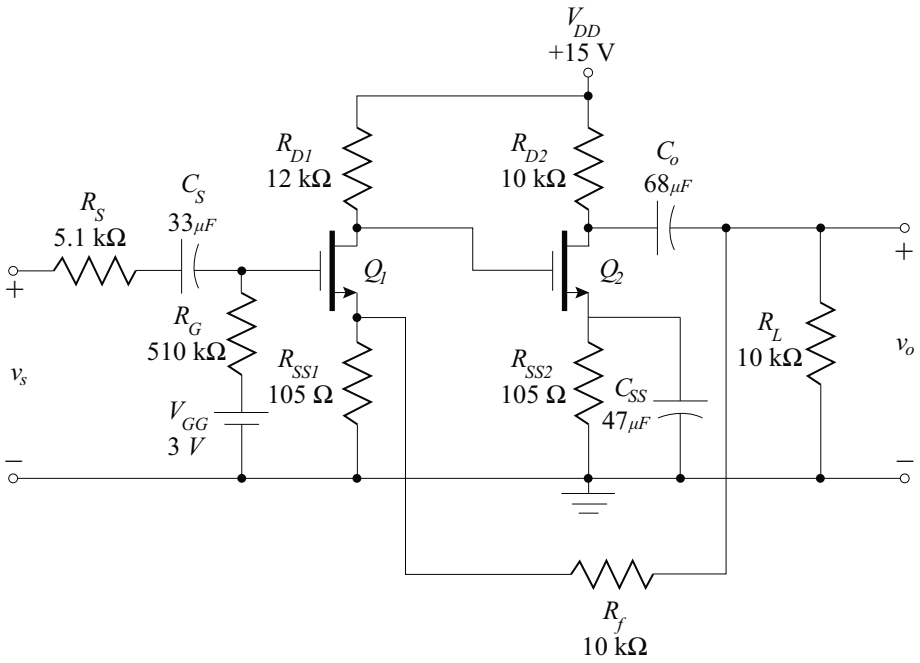
(b) Determine the voltage gain of the circuit without modification.

(c) Rework the design so that the correct voltage gain (20) is attained by changing the feedback (9.1 kΩ) resistor only.



8.29. Determine the closed-loop gain, input resistance, and output resistance of the amplifier shown below. The NMOSFETs are identical with the following characteristic parameters:

$$K = 1.25\,\text{mA/V}^2, \quad V_T = 2\,\text{V}, \quad \text{and} \quad V_A = 120\,\text{V}.$$



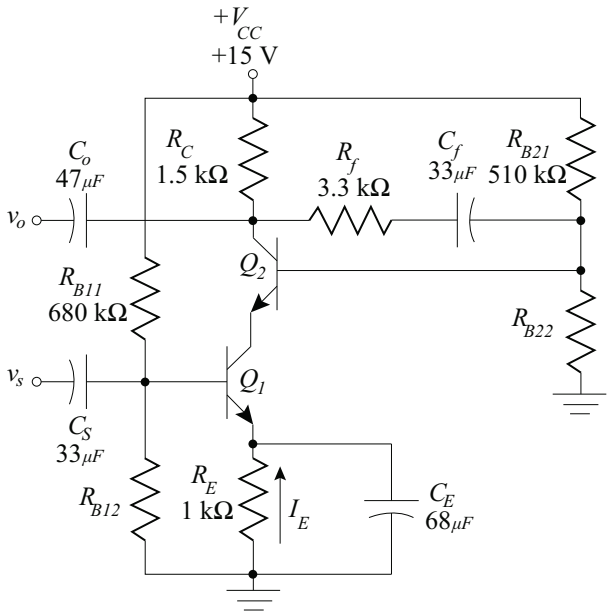
8.30. The BJT cascode amplifier shown below uses identical transistors with the parameters:

$$\beta_F = 200, \quad \text{and} \quad V_A = 200\,\text{V}.$$

(a) Complete the design of the amplifier for $I_E = -2\,\text{mA}$, and $V_{CE1} = V_{CE2} = 5\,\text{V}$. Find the quiescent point of all of the transistors.

(b) Find the closed-loop gain, input resistance, and output resistance of the amplifier.

(c) Confirm the closed-loop gain using SPICE.

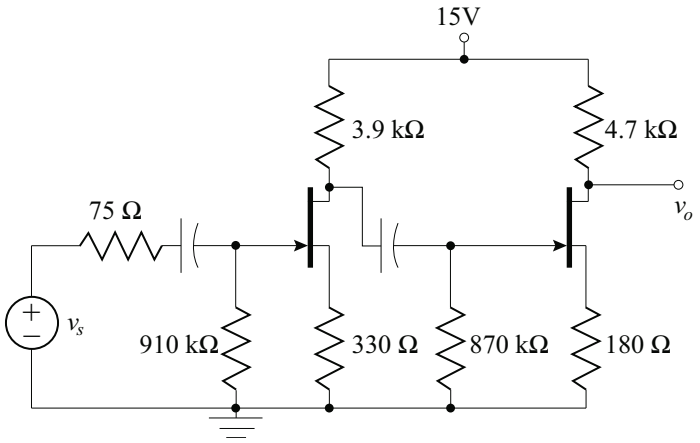


8.31. The amplifier shown is to be used as the basis for a series-shunt feedback amplifier with a voltage gain of twelve (12). The JFETs are described by:

$$V_{PO} = -2\,\text{V}, \quad I_{DSS} = 4\,\text{mA} \quad \text{and} \quad V_A = 200\,\text{V}.$$

(a) Complete the design by inserting a single feedback resistor-capacitor network.

(b) Verify the design using SPICE.



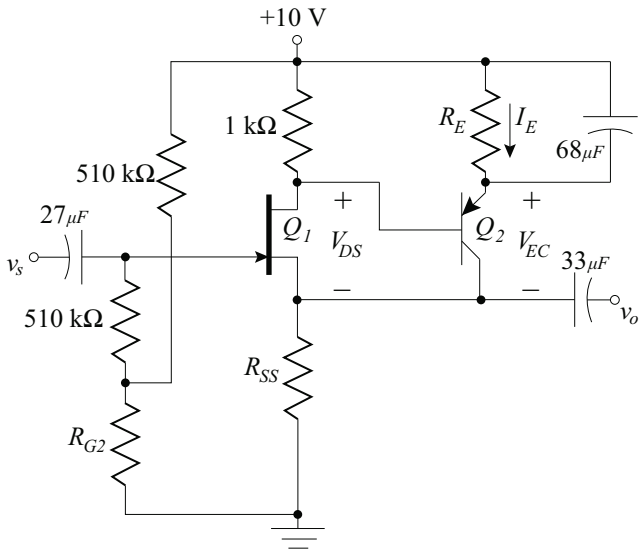
8.32. For the amplifier shown, the transistor characteristics are:

$$\text{JFET:}\quad I_{DSS} = 8\,\text{mA},\quad V_A = 100\,\text{V},\quad V_{PO} = -5\,\text{V},$$
$$\text{BJT:}\quad \beta_F = 200,\quad V_A = 100\,\text{V}.$$

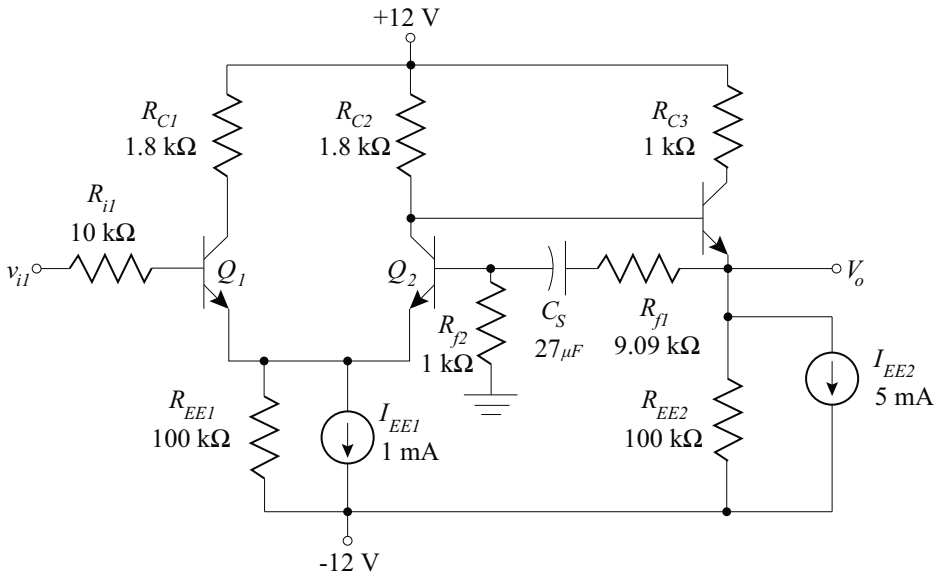
(a) Complete the design of the amplifier for $I_D = 1\,\text{mA}$, $I_E = 3\,\text{mA}$, and $V_{CE} = V_{DS} = 5\,\text{V}$. Find the quiescent point of all of the transistors.

(b) Find the closed-loop gain, input resistance, and output resistance of the amplifier.

(c) Confirm the closed-loop gain using SPICE.



8.33. For the differential amplifier shown, find the closed-loop gain, input resistance, and output resistance of the amplifier. Assume identical transistors with $\beta_F = 120$. Use SPICE to confirm closed-loop gain of the amplifier.

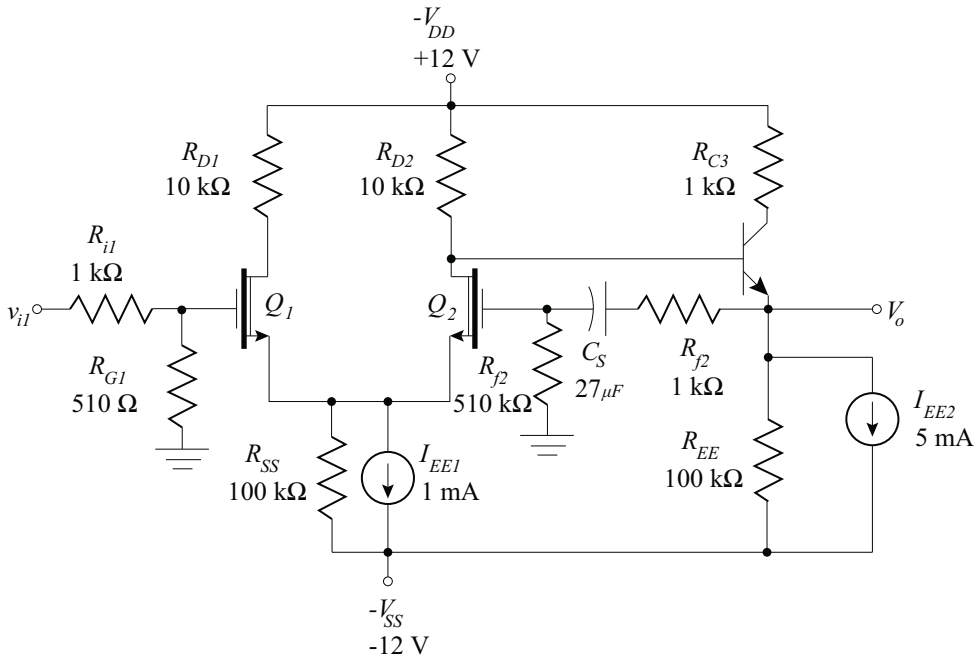


8.34. The transistors in the differential amplifier shown are identical and have the following characteristics:

$$I_{DSS} = 10\,\text{mA}, \quad V_A = 100\,\text{V}, \quad \text{and} \quad V_{PO} = -4.5\,\text{V}.$$

(a) Find the closed-loop gain, input resistance, and output resistance of the amplifier.

(b) Use SPICE to confirm closed-loop gain of the amplifier.



8.35. The series-shunt feedback amplifier of Example 8.5 is to be redesigned to have larger voltage gain. This change is to be accomplished by *alteration of the feedback* (1.2 kΩ) *resistor only*. If the requirement on the midband input resistance, R_{in}, is reduced to:

$$R_{in} \geq 8.80\,\text{k}\Omega\,,$$

from the current value (8.87 kΩ), what is the maximum midband voltage gain that can be achieved?

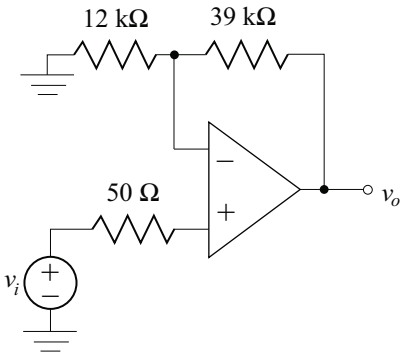
8.36. The performance parameters of the given OpAmp circuit can be determined using feedback techniques. The characteristics of the OpAmp are:

input resistance	- 2 MΩ
output resistance	- 50 Ω
voltage gain	- 800 kV/V

(a) Identify the feedback topology.

(b) Draw a circuit diagram for the loaded basic forward amplifier.

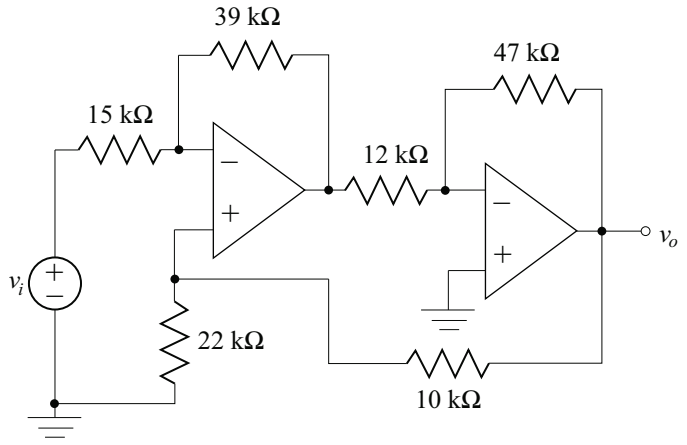
(c) Determine the voltage gain for the total circuit using feedback techniques. Compare results to those determined using the techniques described in Chapter 1 (Book 1).



8.37. Many circuits incorporate both local and global feedback: the simple OpAmp circuit shown is an example of one such circuit. For simplicity, assume the ideal OpAmp expressions derived in Chapter 1 (Book 1) can be used to describe the local feedback characteristics of the amplifier.

(a) Identify the global feedback topology.

(b) Use feedback techniques to determine the overall voltage gain and input resistance of the circuit.



8.38. The characteristics of the amplifier shown include high input resistance with moderate voltage gain and output resistance. It is desired to reduce the output resistance of the amplifier through the use of feedback without significantly altering the input resistance.

The transistors in the circuit have parameters:

$$I_{DSS} = 2.5\,\text{mA}, \quad V_{PO} = -2.5\,\text{VA} = 100\,\text{V}, \quad \text{and} \quad \beta_F = 150\,V_A = 200\,\text{V},$$

the quiescent conditions have been found to be:

$$|I_{DQ}| = 2.10\,\text{mA} \qquad V_{DSQ} = 14.7\,\text{V}, \tag{8.62}$$

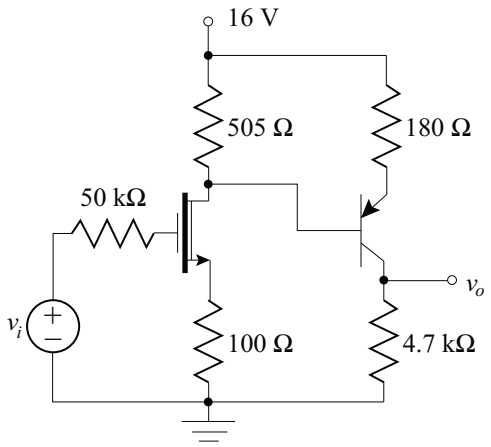
$$|I_{CQ}| = 1.95\,\text{mA} \qquad V_{CEQ} = -6.49\,\text{V}. \tag{8.63}$$

(a) What feedback topology will lower the output resistance while maintaining high input resistance?

(b) Design a feedback network that will meet the following design goals:

- Transistor quiescent conditions are not changed.
- voltage gain no less than 10.
- minimal output resistance.

(c) Determine the output resistance of the amplifier designed in part (b).



8.39. For the feedback amplifier shown, the Silicon transistors are described by:

$$\beta_F = 120.$$

Assume v_i has zero DC component.

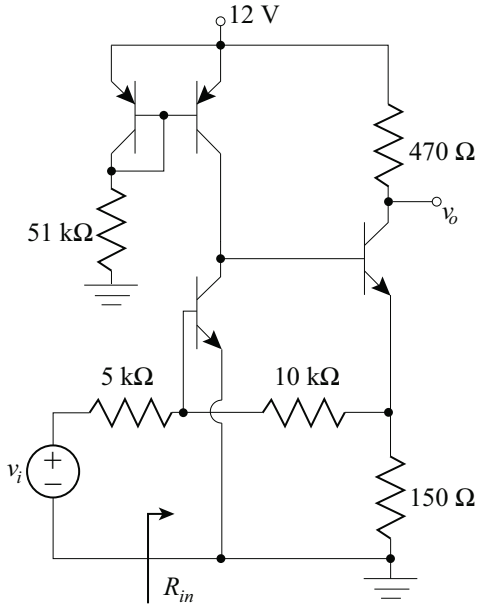
(a) Identify the feedback topology.

(b) Determine the quiescent conditions.

(c) Determine the voltage gain,

$$A_V = \frac{v_o}{v_i}.$$

(d) Determine the input resistance, R_{in}.



8.40. For the feedback amplifier shown, the Silicon transistors are described by $\beta_F = 100$.

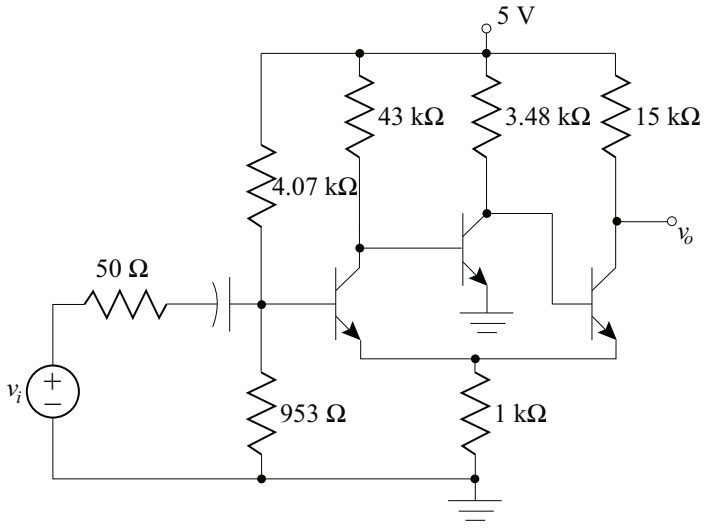
(a) Identify the feedback topology.

(b) Determine the quiescent conditions.

(c) Determine the voltage gain,

$$A_V = \frac{v_o}{v_i}.$$

(d) Verify the results of parts (b) and (c) using SPICE.



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Thomas Schubert received BS, MS, and PhD degrees in Electrical Engineering from the University of California at Irvine (UCI). He was a member of the first engineering graduating class and the first triple-degree recipient in engineering at UCI. His doctoral work discussed the propagation of polarized light in anisotropic media.

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